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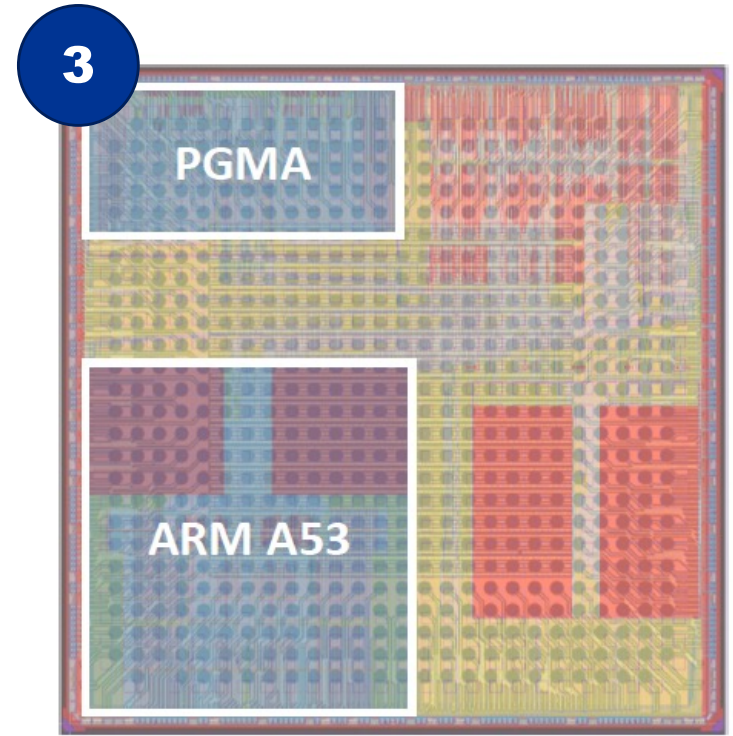
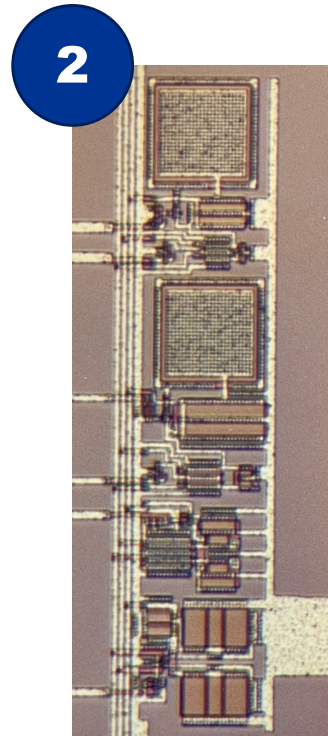
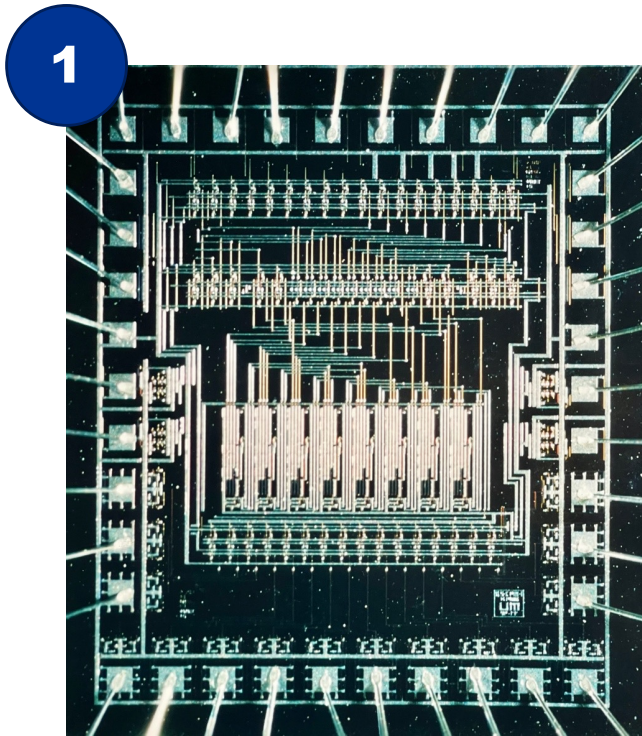
cadence®

**Doing EDA in Disruptive
Times: Reflections on
Analog and AI**

Rob A. Rutenbar

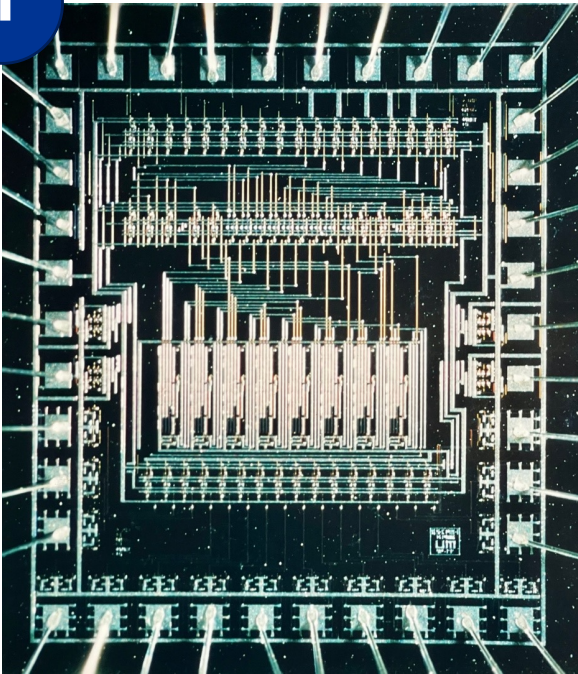
Senior Vice Chancellor for Research
Distinguished Professor of CS & ECE
University of Pittsburgh

A Talk in 3 Disruptions (3 Chips)



Disruption #1

1

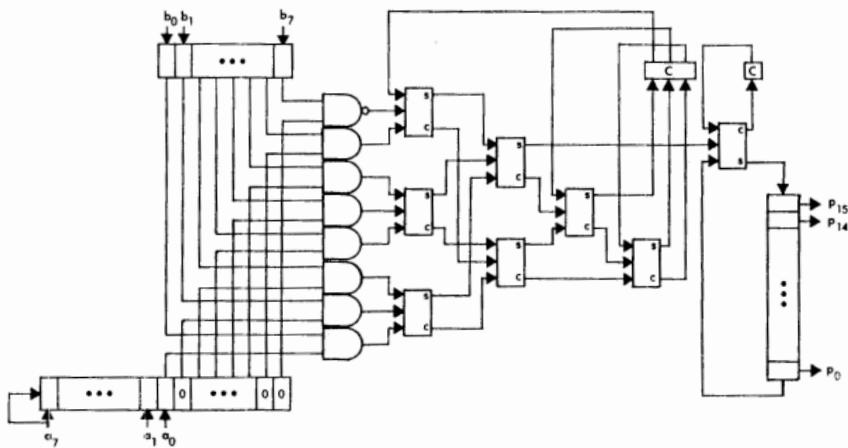


~1980

- $\lambda = 4\mu\text{m}$
- Depletion-mode NMOS
- Single metal
- 503 transistors
- 200KHz
- Fabled by General Motors

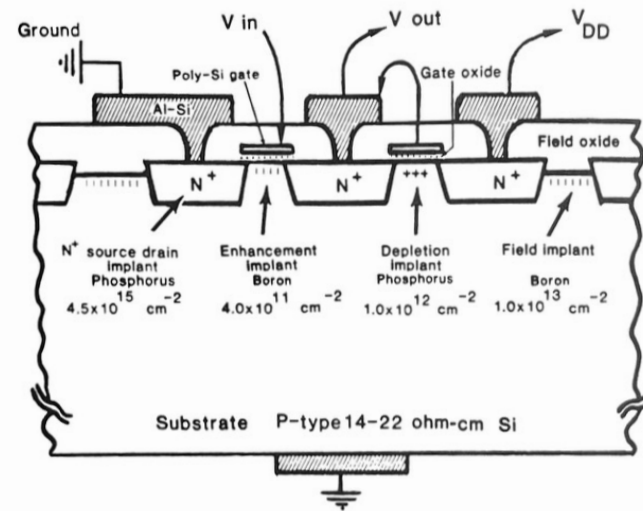
Disruption #1

- Multiply-Add Circuit



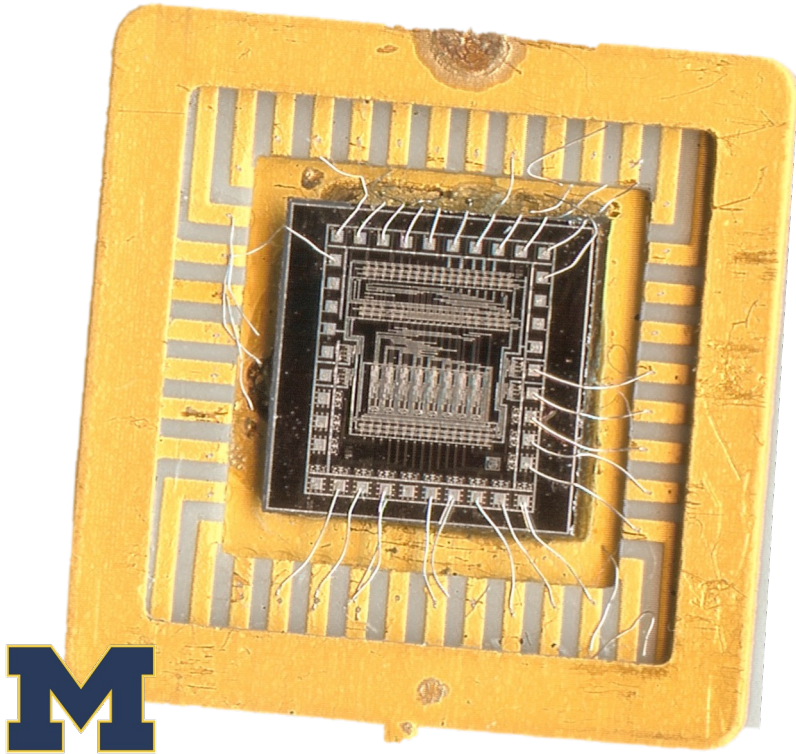
< 100 gates

- Technology



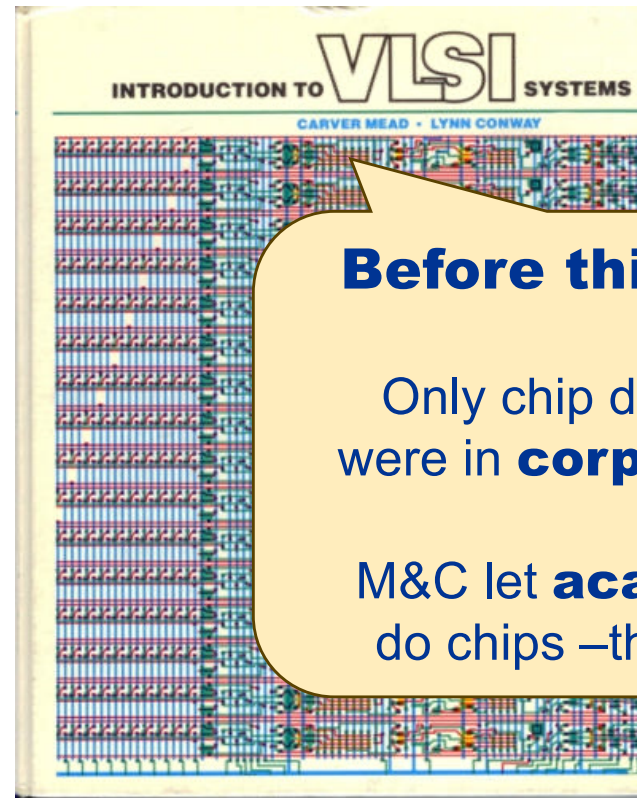
4000nm node (~1/2-CMOS)

Disruption #1: Mead & Conway



M

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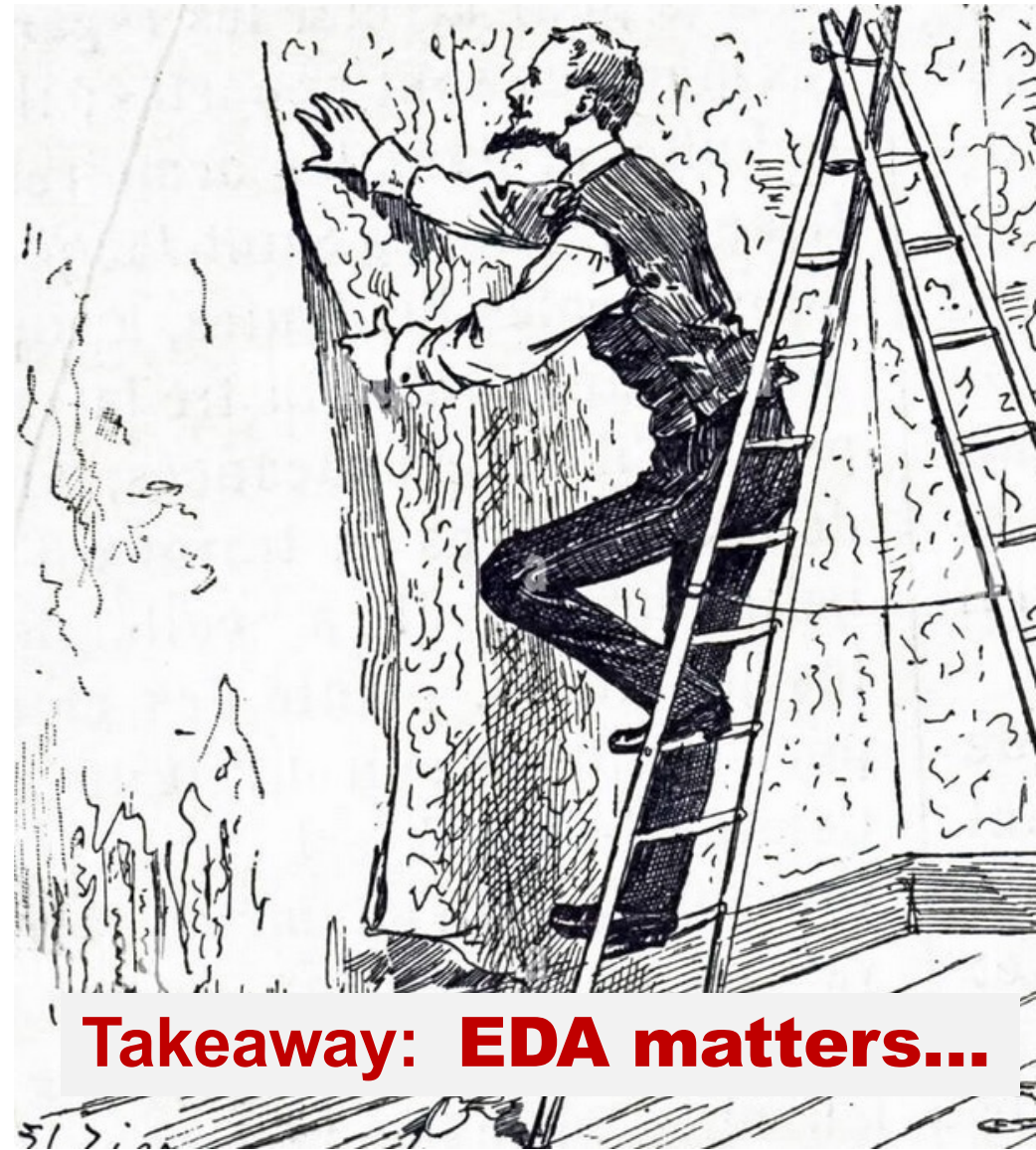
Before this book:

Only chip designers
were in **corporations**

M&C let **academics**
do chips –then **EDA**

~1980 Design Methodology & Toolchain

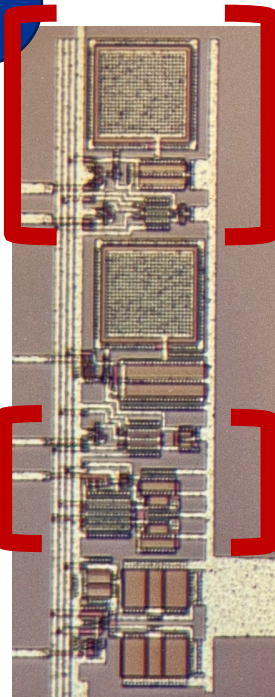
- Ladder
- Line-printer
- Masking tape
- Sharpie
- DRC checker
- BSD Unix "vi" editor



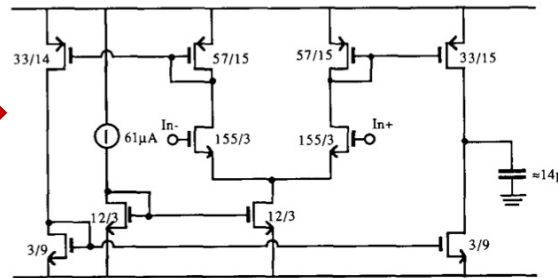
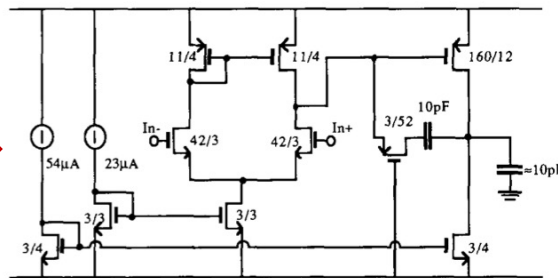
Takeaway: EDA matters...

Disruption #2

2



OTA opamp



2-Stage opamp

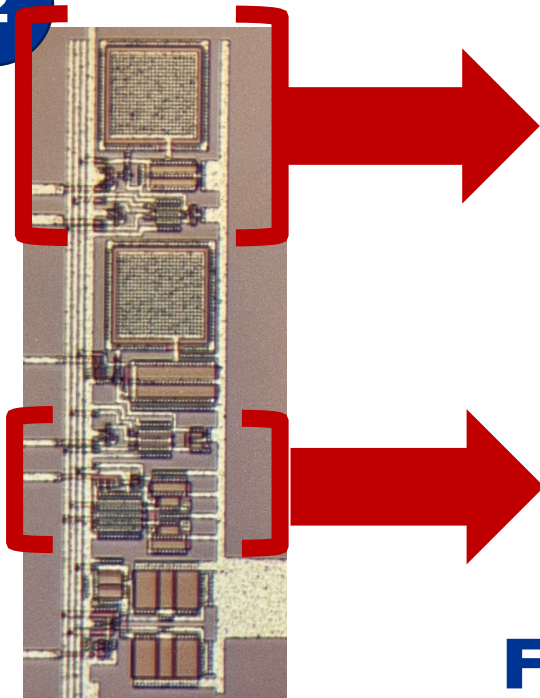
INPUT SPECIFICATIONS AND RESULTS FOR FABRICATED OP AMPS

Parameter	Units	Circuit OTA-1			Circuit 2Stage-1		
		Spec	SPICE Results	Chip Results	Spec	SPICE Results	Chip Results
Gain	dB	≥ 60	60	69.5	≥ 45	45.2	48.4
Unity Gain Freq.	MHz	≥ 1.0	1.25	0.993	≥ 2.8	2.52	2.6
Phase Margin	Deg.	≥ 45	46	43	≥ 60	82	85
Load Capacitance	pF	10	10	~ 14	14	14	~ 14
Supply	V	± 2.5	± 2.5	± 2.5	± 2.5	± 2.5	± 2.5
Slew Rate	V/μS	≥ 2.0	2.1	-1.6/+2.0	≥ 2.5	2.42	-3.0/+4.5
Power	mW	≤ 3.0	0.63	0.62	-	0.56	0.56
Input Offset	mV	-	6.6	11.4	-	16	18.4

1988
3μm CMOS

Disruption #2: Algorithmic Analog EDA

2



**First synthesized circuits
from the CMU analog tools**

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Broader Disruption: *Algorithmic EDA*

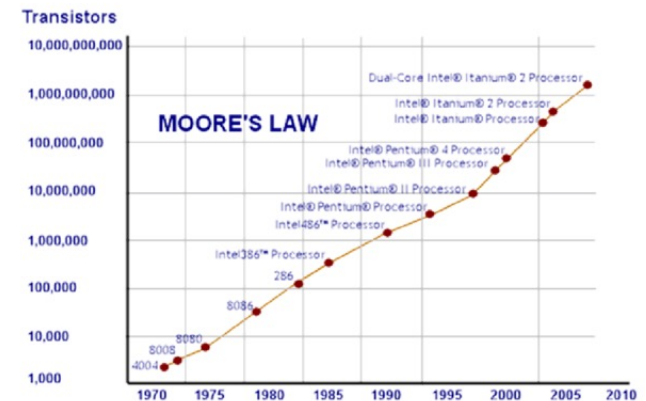
Twin disruptions of 1980s, 90s

- **Moore's law**

- Exponentially better, cheaper **hardware**

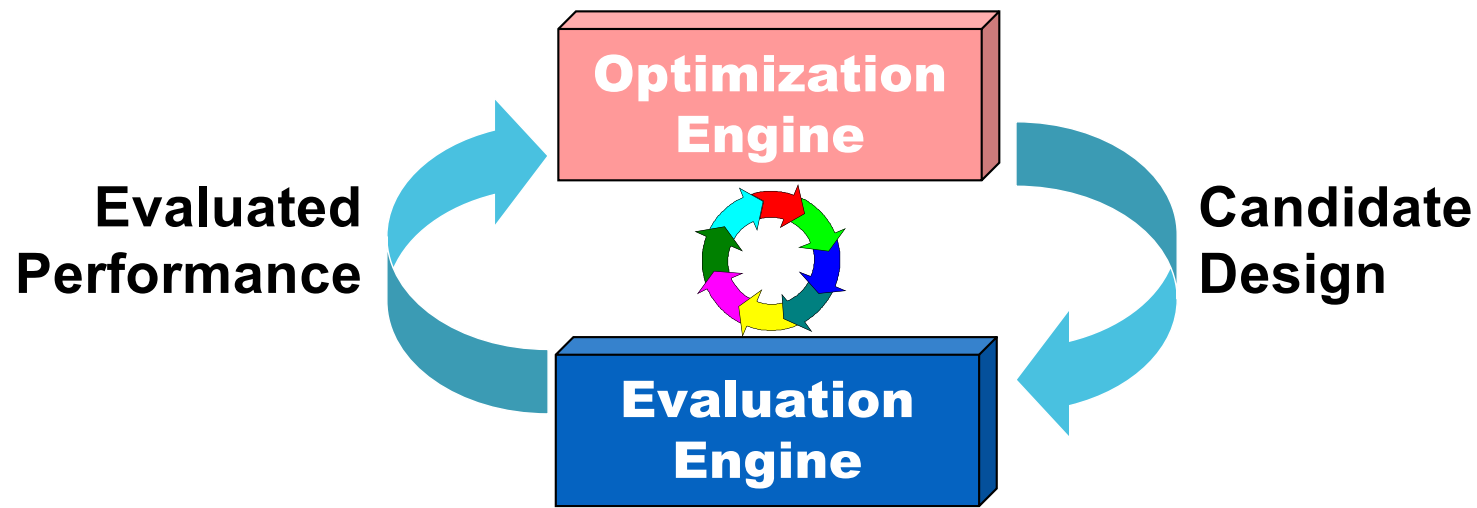
- **Rise of algorithms**

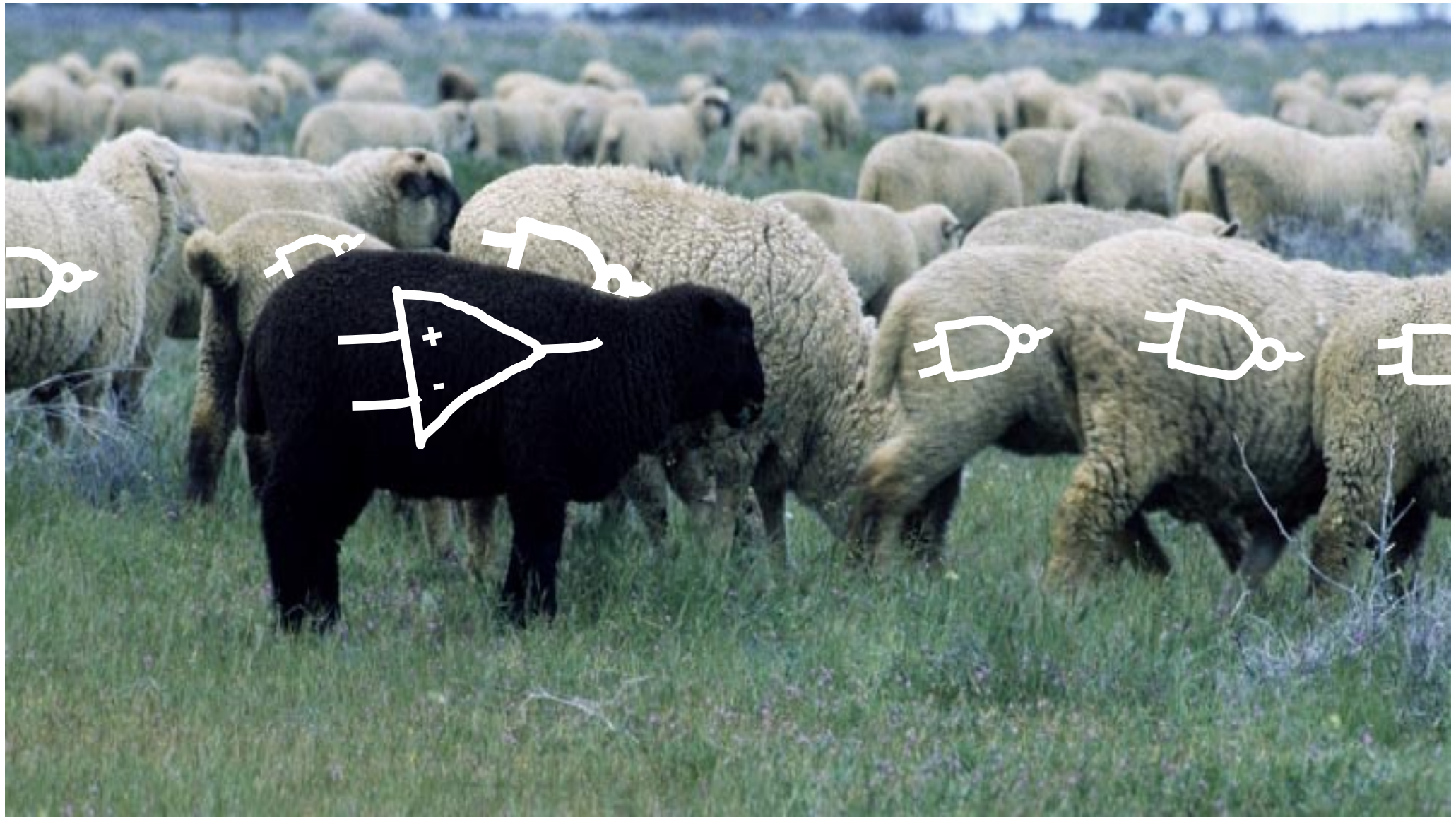
- Model problems **formally, with principled goals**
- Measure, approximate **circuit results, inside algorithms**
- Focus on **accuracy, complexity & efficiency**
- **We apply ideas from optimization**



Synthesis = Algorithms + Optimization

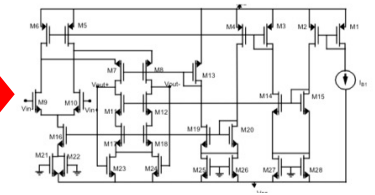
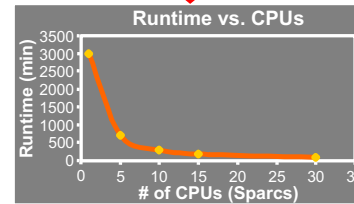
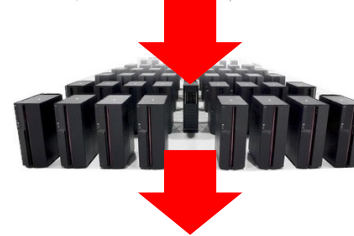
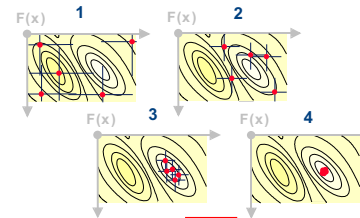
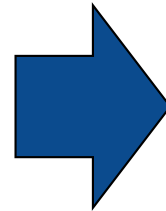
- Smart models & engines to support **principled search** for best design to **meet designer constraints**



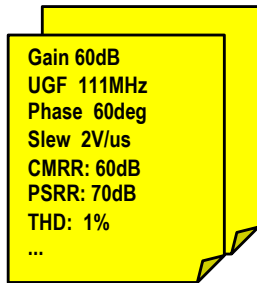


Analog EDA: Fundamental Debate

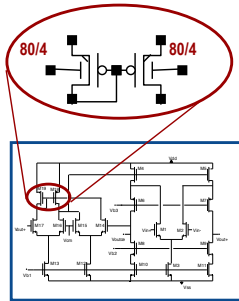
- Analog – it's art, mysterious, all **patterns in my head**
- Nope – it's **optimization**: big hard optimization



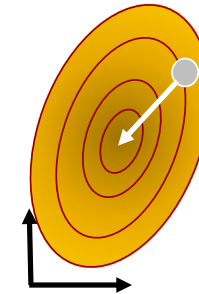
Landscape of “Core” Analog Tools



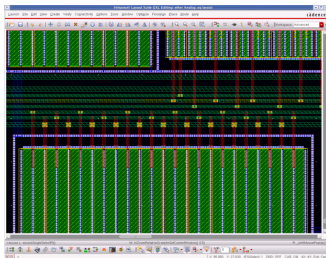
Constraint Capture



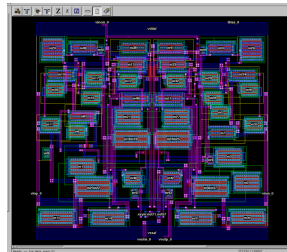
Sizing & Biasing



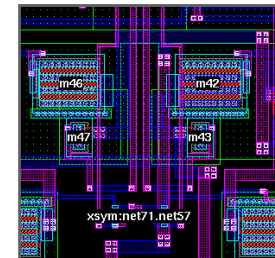
Yield Optimization



Device Gen



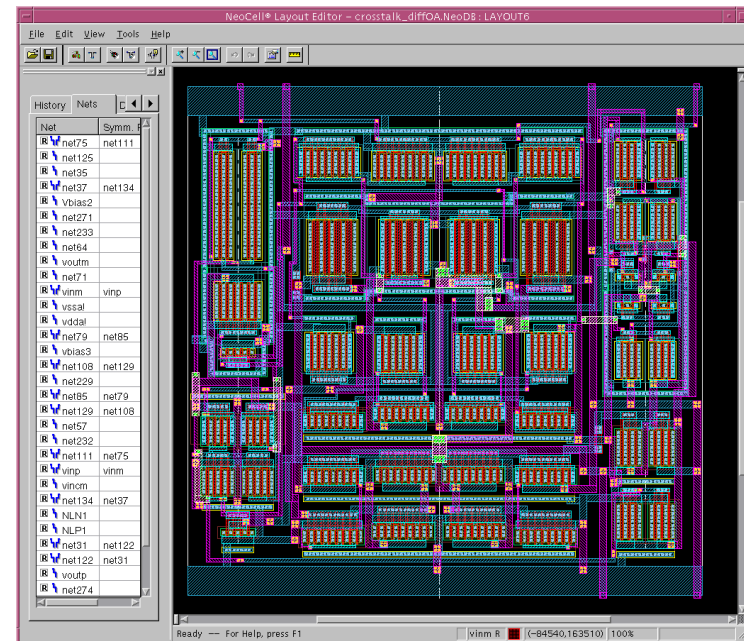
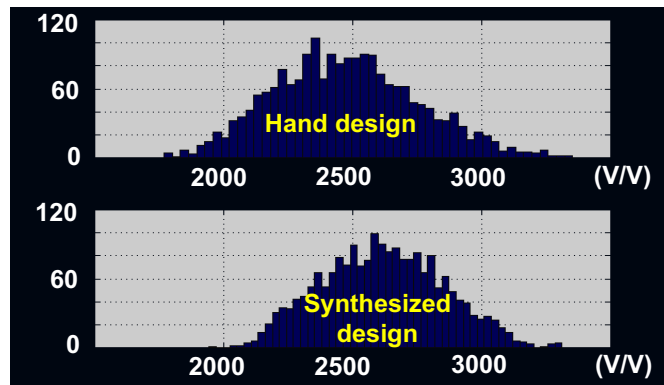
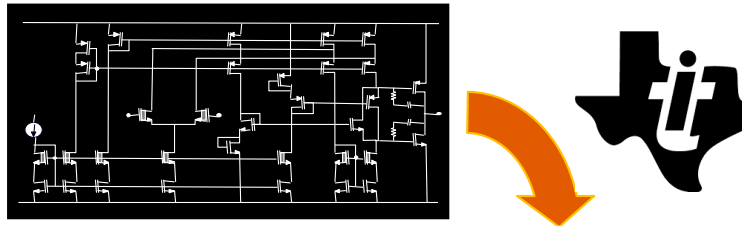
Placement



Routing

Two (Historical) Analog Examples

- Practical Spice-in-the-Loop optimizers for sizing/biasing
- Automatic layouts with both aesthetics & performance



Looking Back....



What did we get **right?**
We did we get **wrong?**

Simplify All EDA into 2-Dim Space

- **Claim***: There are only 2 kinds of EDA tools

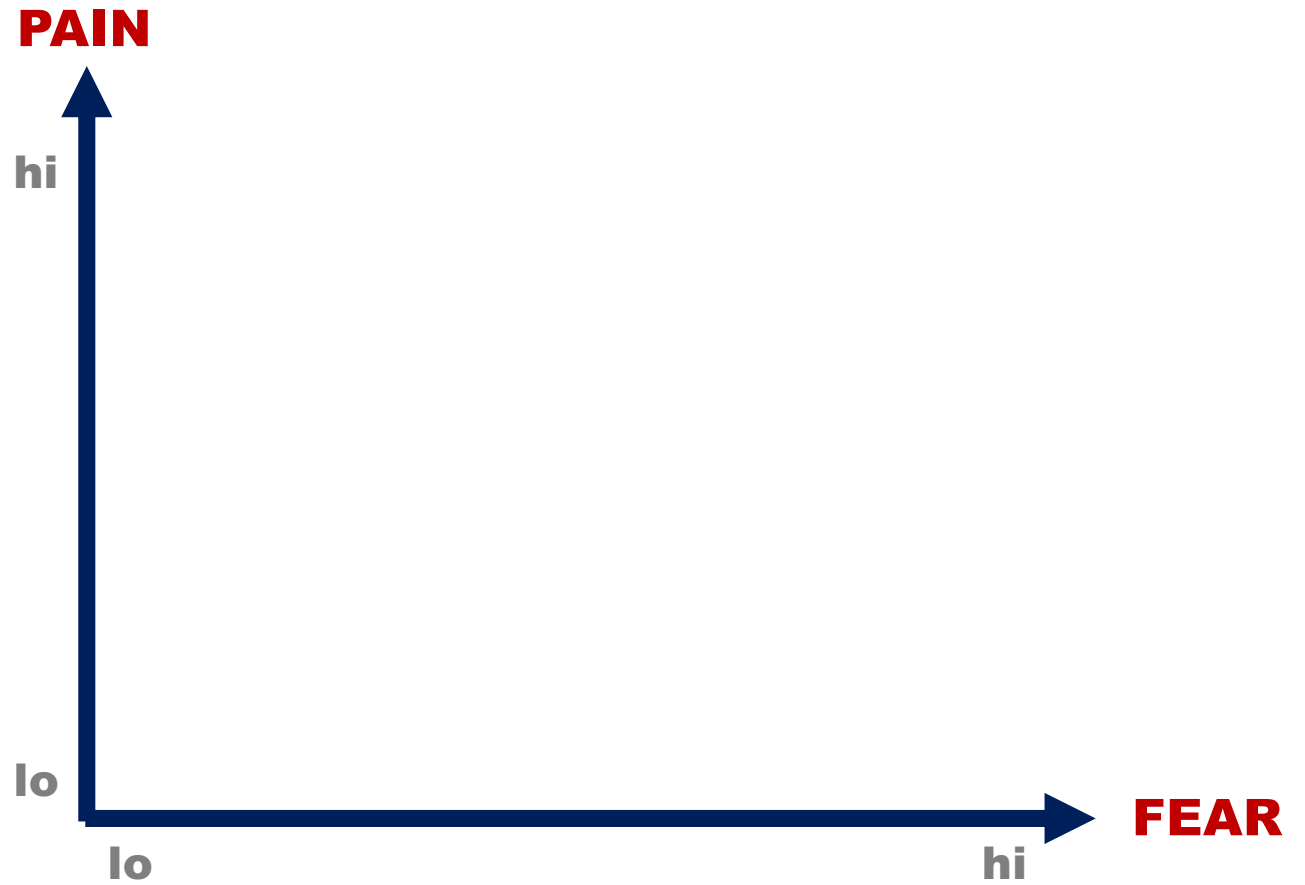


INSURANCE

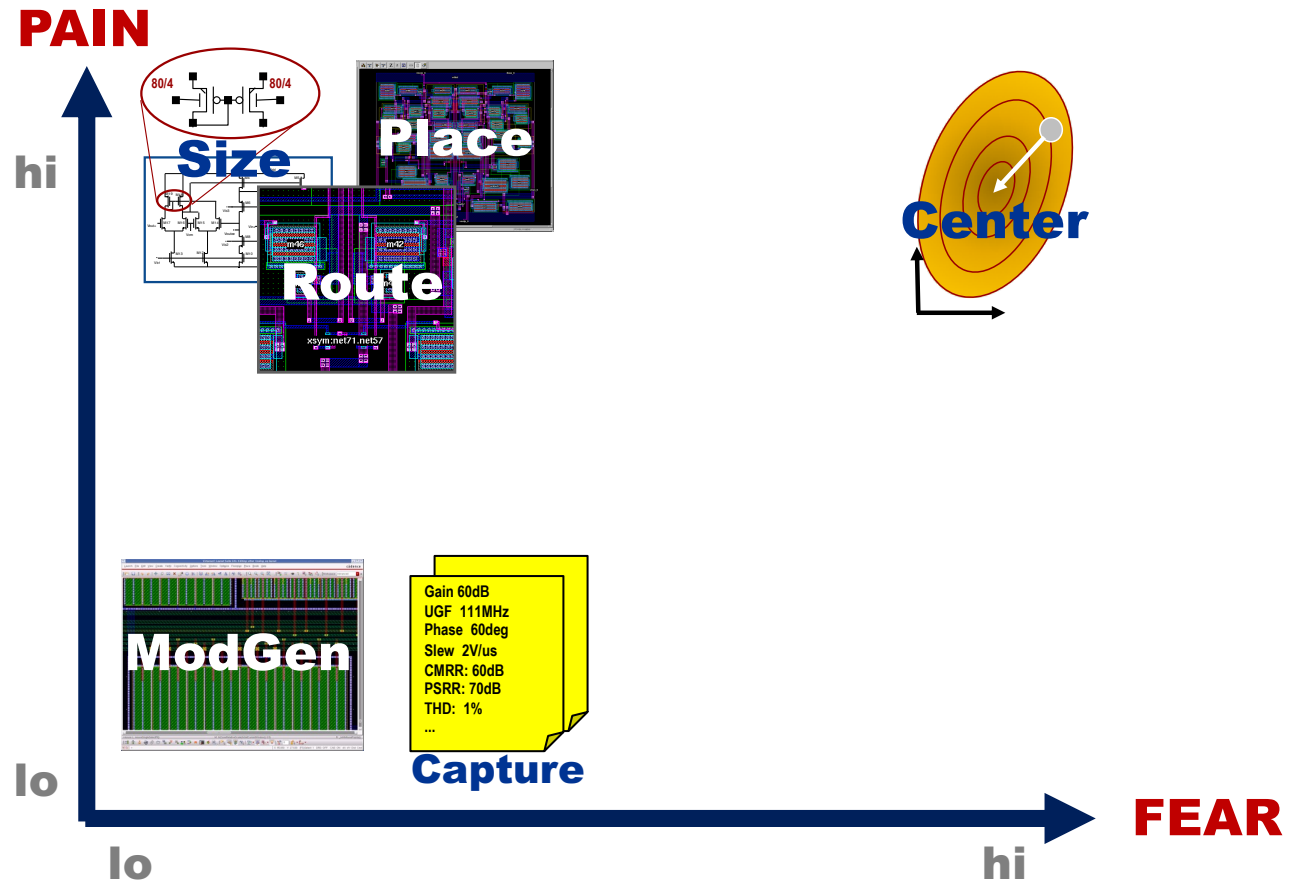


PAIN RELIEF

Analog EDA on Pain/Fear Plot



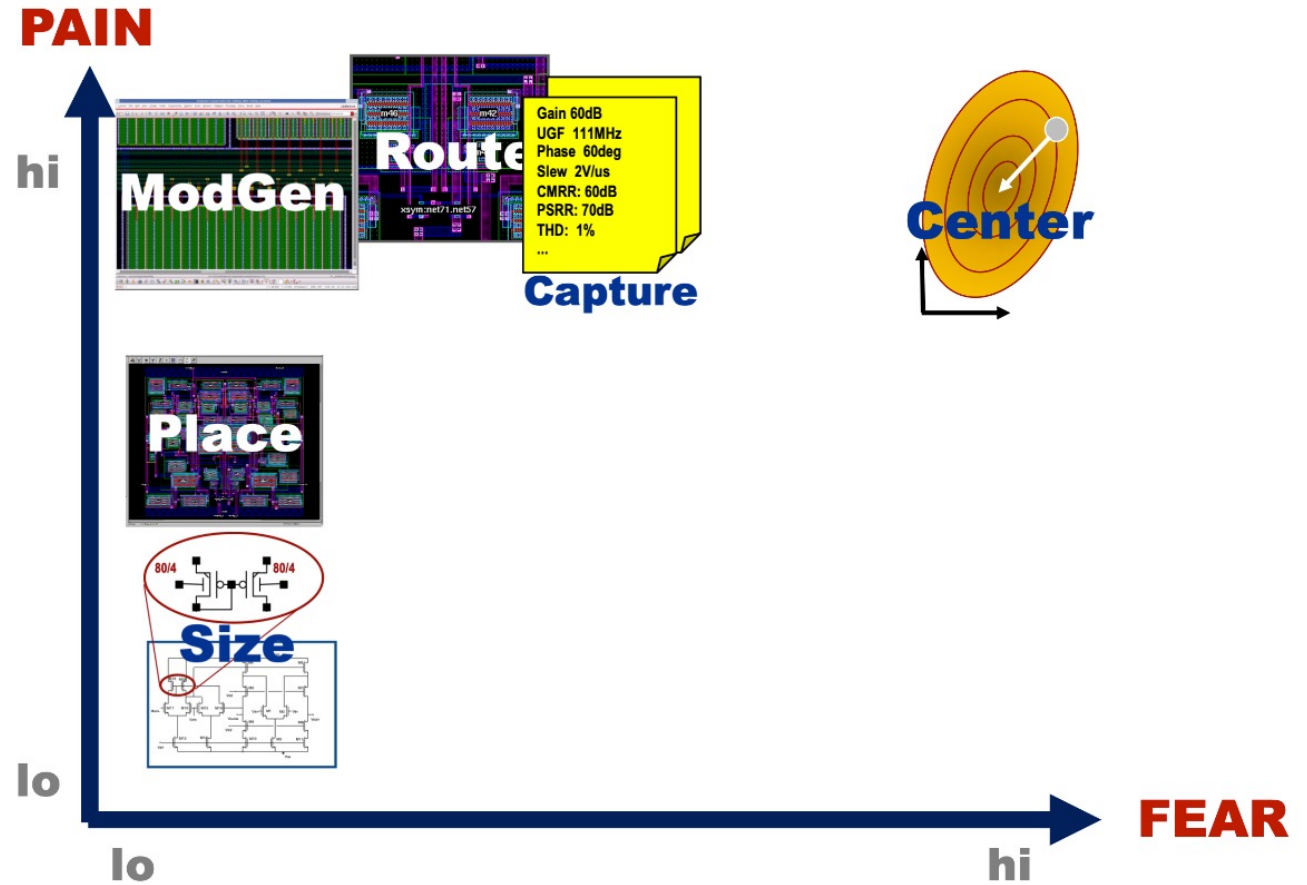
Analog EDA on Pain/Fear Plot



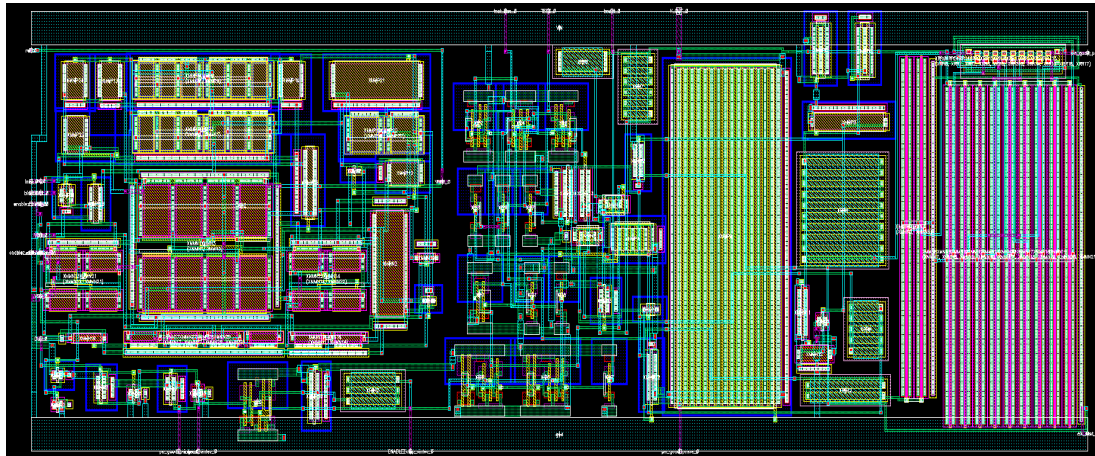
Analog EDA on Pain/Fear Plot

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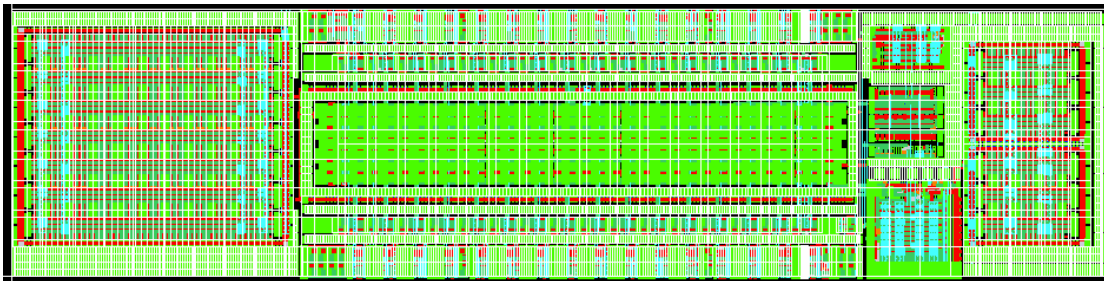


Aside: Enduring Role of MODGEN



250nm
Place ~ floorplan

In either case,
nobody wants to
draw device shapes
all by hand



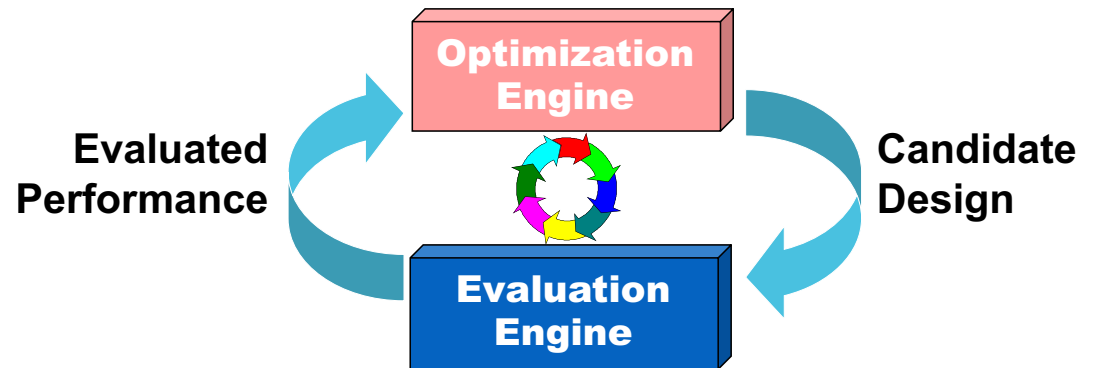
14nm
Place ~ fixed grid

Teaser for Final Part of Talk

- Analog – expert

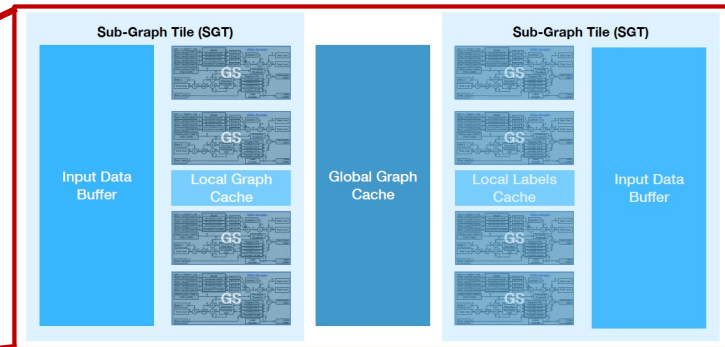
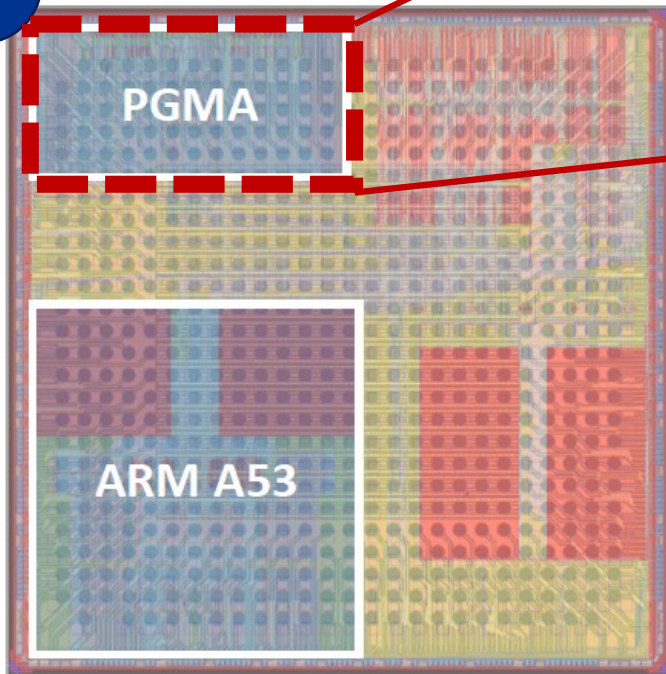


- Analog – optimizer



Disruption #3

3



2020

A 3mm² Programmable Bayesian Inference Accelerator for Unsupervised Machine Perception using Parallel Gibbs Sampling in 16nm

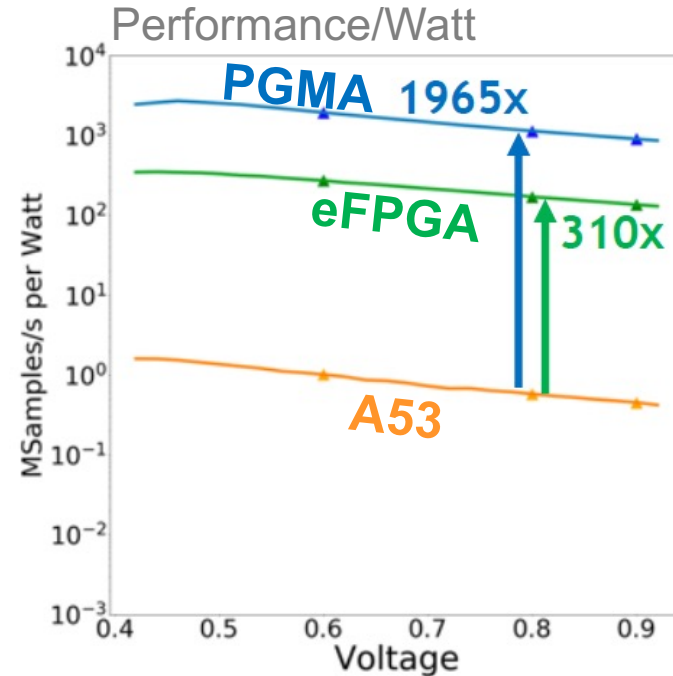
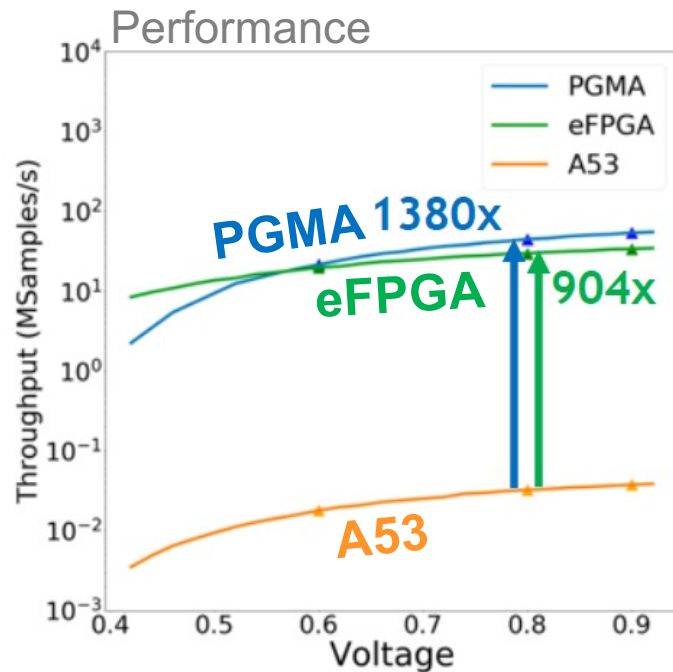
Glenn G. Ko¹, Yuji Chai¹, Marco Donato¹, Paul N. Whatmough^{1,2}, Thierry Tamba¹,
Rob A. Rutenbar³, David Brooks¹, Gu-Yeon Wei¹

¹Harvard University, MA, ²Arm Research, MA, ³University of Pittsburgh, PA

- TSMC 16nm FFC
- ~2M gates, 450MHz
- Part of a larger SOC experiment at Harvard called **SM5: ML for IOT**

PGMA vs Arm53 vs eFPGA (on SOC)

- **PGMA: 1000X+ throughput vs CPU; 6X+ ops/W vs eFPGA**



Key Takeaways

- The world **changed** fundamentally in 2012
- **AI** is invading everything, everywhere (even Rob...)
- Even **EDA...**

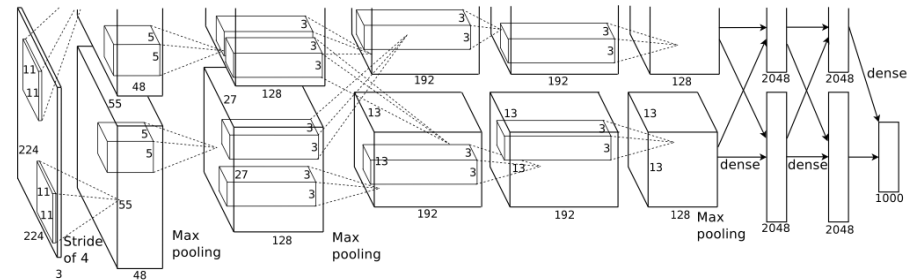
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ImageNet Classification with Deep Convolutional Neural Networks

Alex Krizhevsky
University of Toronto
kriz@cs.utoronto.ca

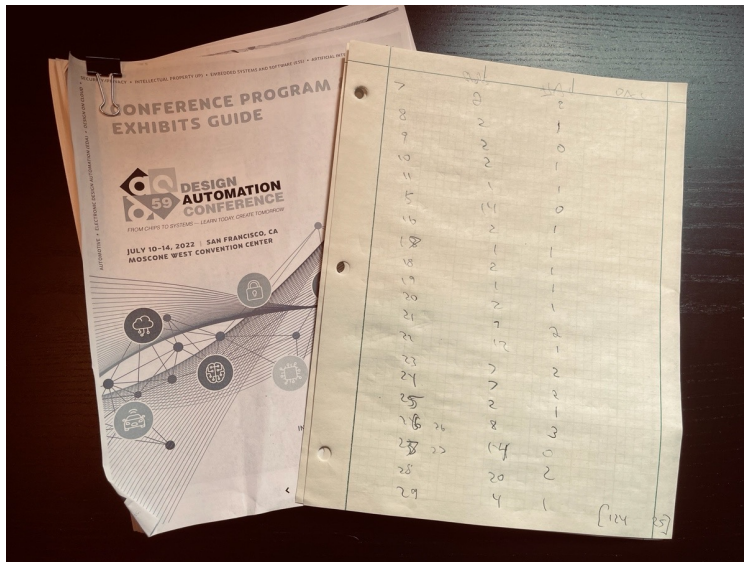
Ilya Sutskever
University of Toronto
ilya@cs.utoronto.ca

Geoffrey E. Hinton
University of Toronto
hinton@cs.utoronto.ca

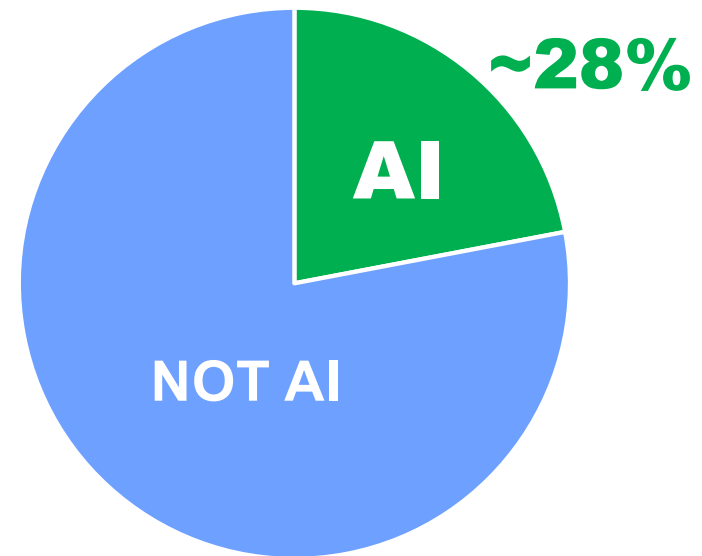


NIPS 2012

Quantifying AI in EDA: DAC22



DAC22 program: Count every talk, tutorial, poster, slot, that mentions **AI, ML, deep nets...**



836 DAC event slots

A 3D grid of white cubes, with a single red cube in the center. The cubes are arranged in a regular pattern, and the red cube stands out prominently.

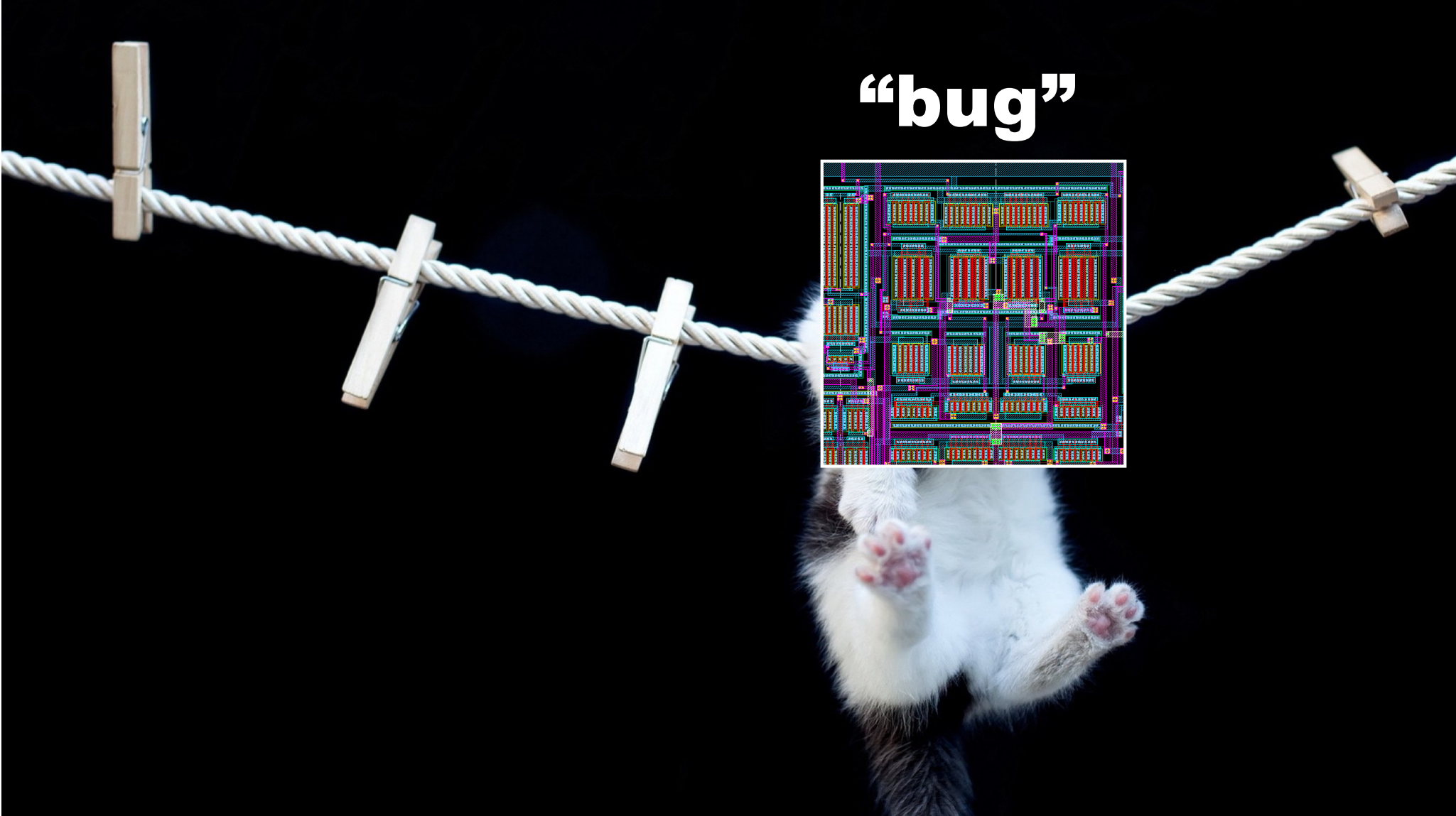
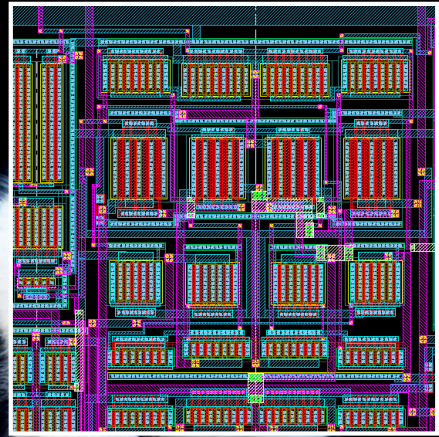
**AI = Statistical regression,
in high-dimensional spaces...**

...to find low-dimensional patterns

“cat”



“bug”

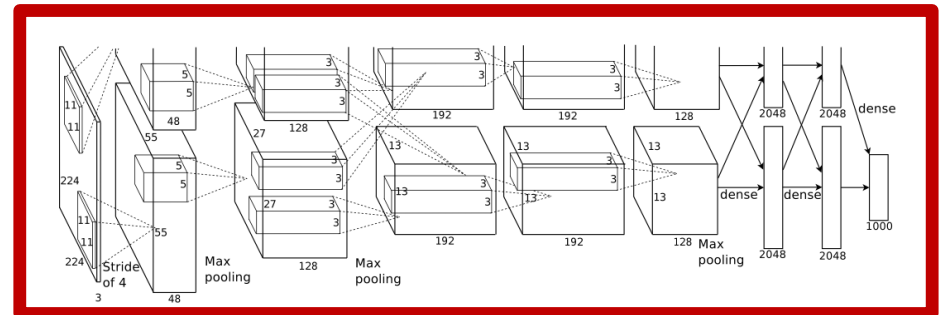
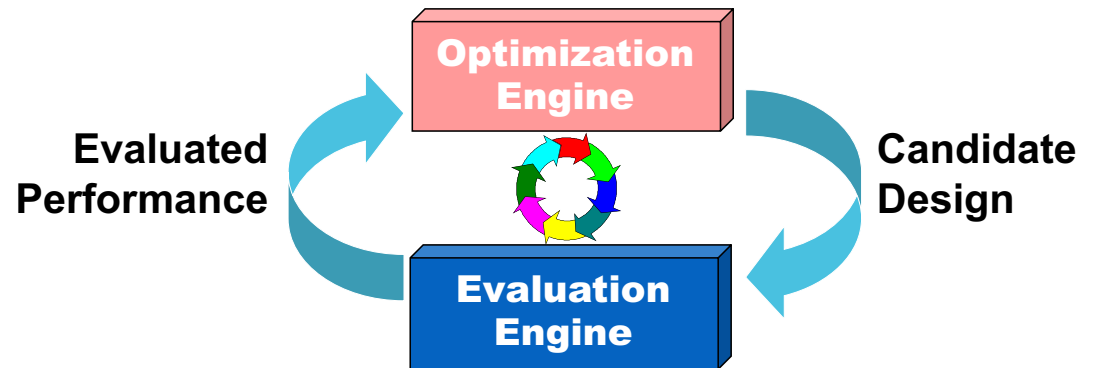


Analog and AI, Revisited

- Analog – expert



- Analog – optimizer & deep patterns



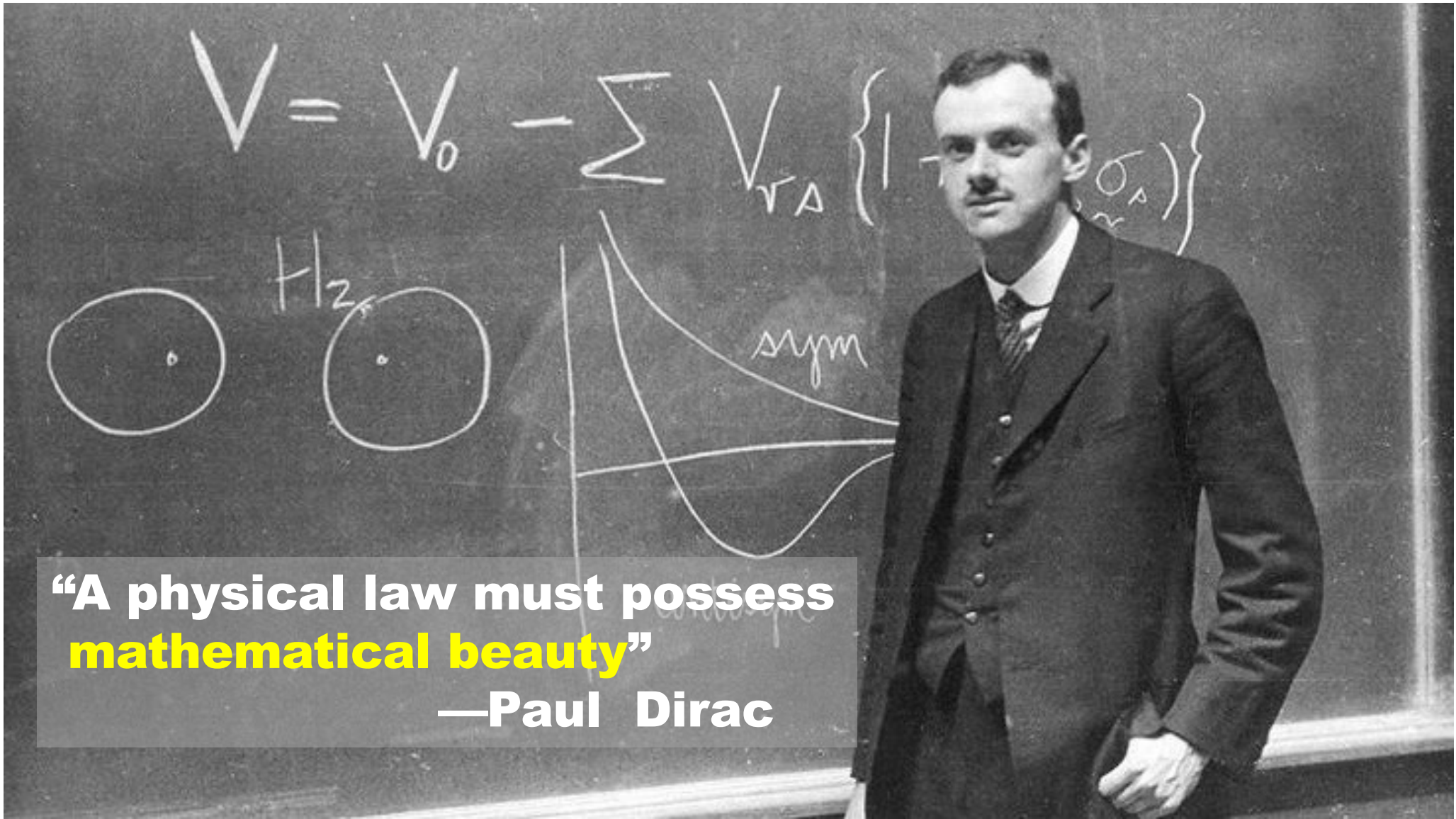
Analog as “Operationalized Patterns”

”This is ugly”

“This is not what
I had in mind”



Fundamental truth about analog:
Aesthetics often a **surrogate** for correctness

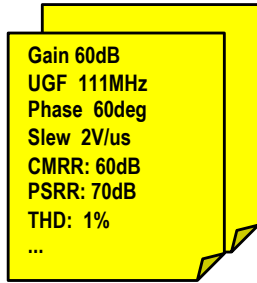


“A physical law must possess
mathematical beauty”

—Paul Dirac

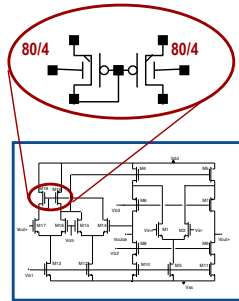
AI Meets “Core” Analog Tools...?

AI



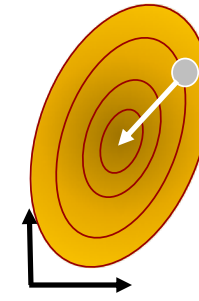
Capture

AI



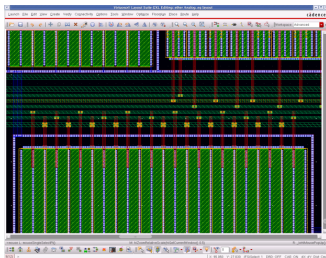
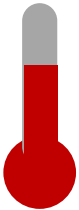
Sizing

AI



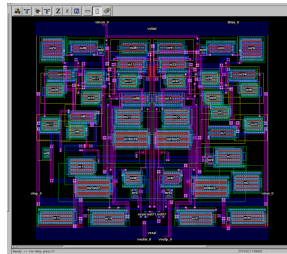
Center

AI



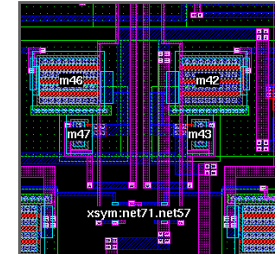
ModGen

AI



Place

AI



Route

Digital Ex: AI Meets Floorplanning



Article

A graph placement methodology for fast chip design

<https://doi.org/10.1038/s41586-021-03544-w>

Received: 3 November 2020

Accepted: 13 April 2021

Published online: 9 June 2021

Azalia Mirhoseini^{1,4,5*}, Anna Goldie^{1,3,4,5*}, Mustafa Yazgan², Joe Wenjie Jiang¹, Ebrahim Songhor¹, Shen Wang¹, Young-Joon Lee², Eric Johnson¹, Omkar Pathak², Azade Nazi¹, Jiwoo Pak², Andy Tong², Kavya Srinivasa², William Hang¹, Emre Tuncer², Quoc V. Le¹, James Laudon¹, Richard Ho², Roger Carpenter² & Jeff Dean¹

NEWS AND VIEWS | 09 June 2021

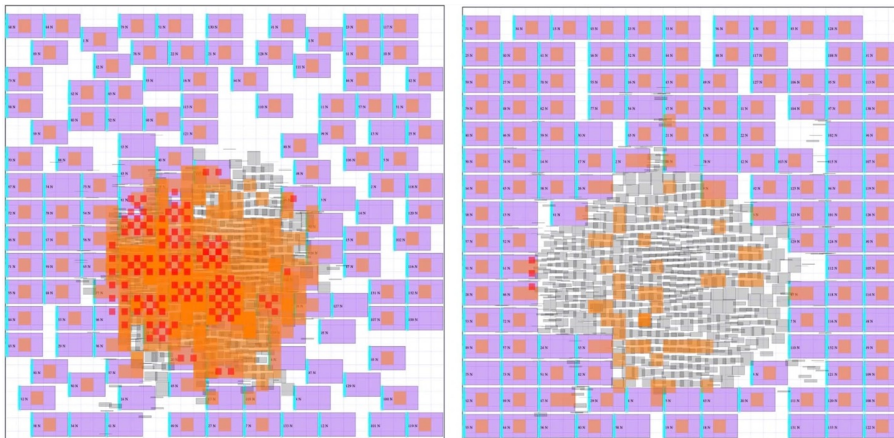
AI system outperforms humans in designing floorplans for microchips

A machine-learning system has been trained to place memory blocks in microchip designs. The system beats human experts at the task, and offers the promise of better, more-rapidly produced chip designs than are currently possible.

EDITORIAL | 09 June 2021

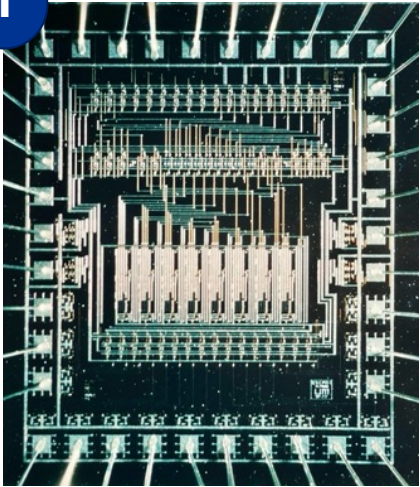
Google's AI approach to microchips is welcome – but needs care

Artificial intelligence can help the electronics industry to speed up chip design. But the gains must be shared equitably.

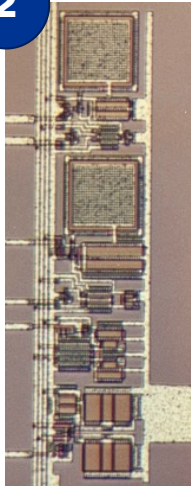


Bonus Disruption...

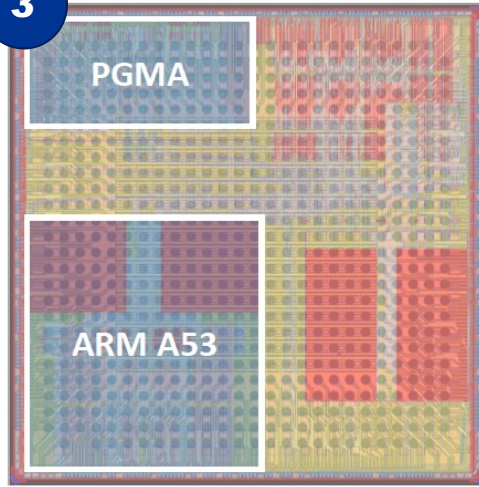
1



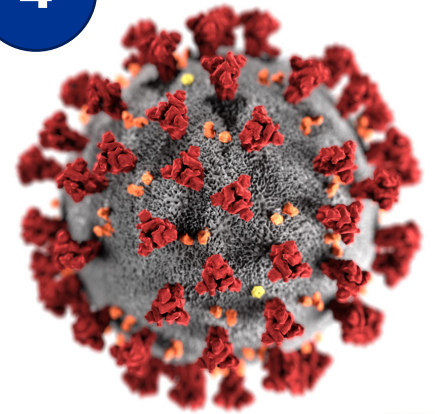
2



3



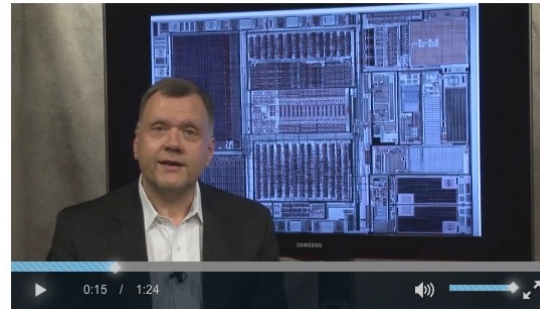
4



VLSI CAD MOOCs



- Since 2013, I'm running MOOCs on **VLSI CAD**



Example: 4 pads + Bigger 5-gate Netlist

$C = \begin{pmatrix} 0 & 1 & 1 & 0 & 0 \\ 1 & 0 & 1 & 1 & 1 \\ 1 & 0 & 1 & 0 & 1 \\ 0 & 1 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 0 \end{pmatrix}$ $A = \begin{pmatrix} 21 & -1 & -10 & 0 & 0 \\ -1 & 4 & -1 & -1 & -1 \\ -10 & -1 & 13 & -1 & 0 \\ 0 & -1 & -1 & 4 & -1 \\ 0 & -1 & 0 & -1 & 3 \end{pmatrix}$

$b_x = \begin{pmatrix} 0 \\ 0 \\ 1 \\ 1 \\ 0.5 \end{pmatrix}$ $b_y = \begin{pmatrix} 10 \\ 0 \\ 0 \\ 1 \\ 0 \end{pmatrix}$

All wire weights = 1 except two highlighted: gate1 to pad, gate1 to gate2

Slide 64 © 2013, R.A. Rutenbar

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ILLINOIS

VLSI CAD: Logic to Layout

Rob A. Rutenbar

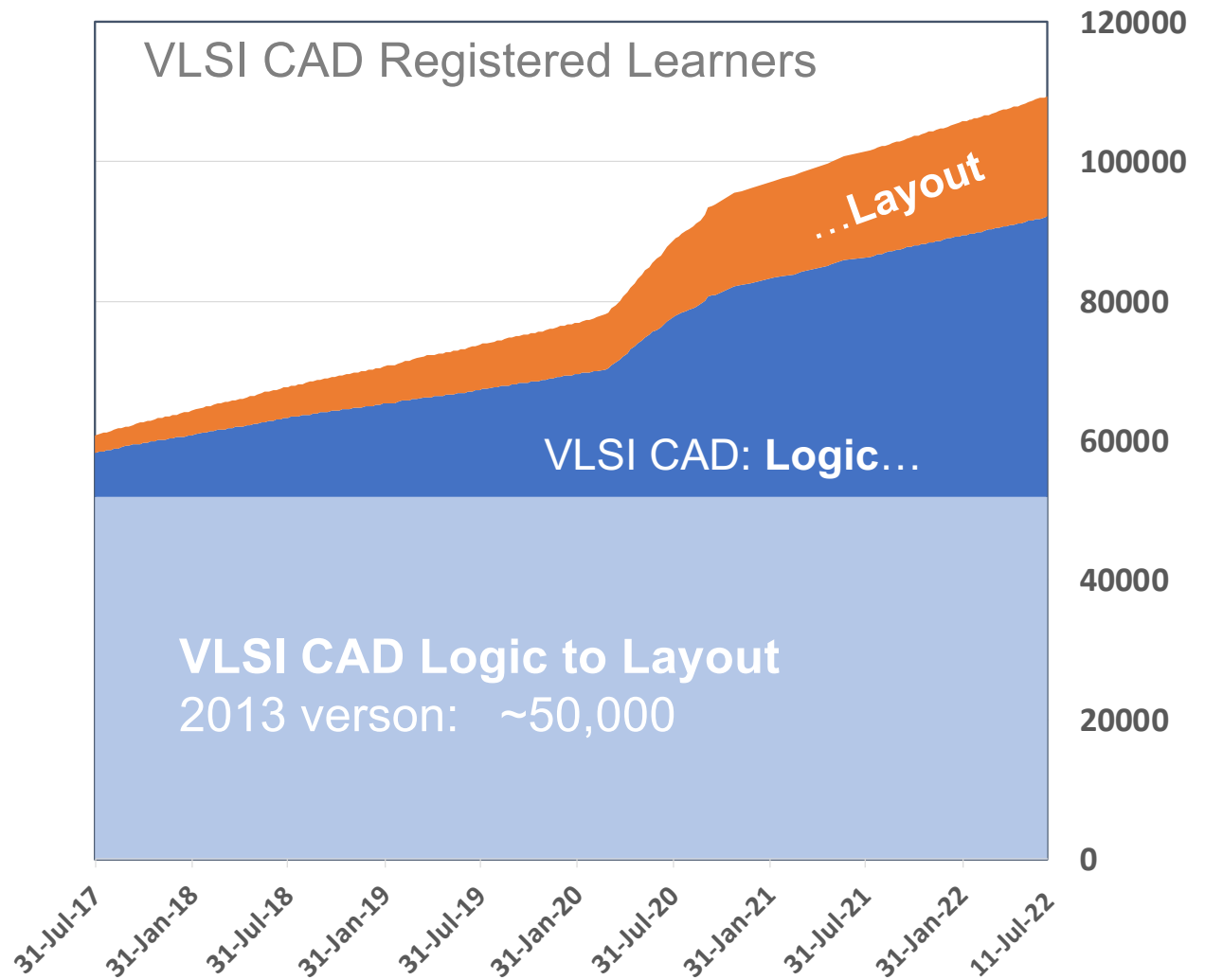
A modern VLSI chip has a zillion parts -- logic, control, memory, interconnect, etc. How do we design these complex chips? Answer: CAD software tools. Learn how to build these tools in this class.

Workload: 10-12 hours/week

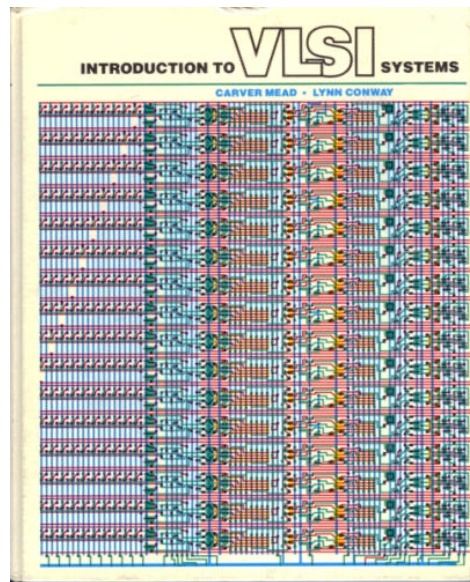
Chris Knapton/Digital Vision/Getty Images

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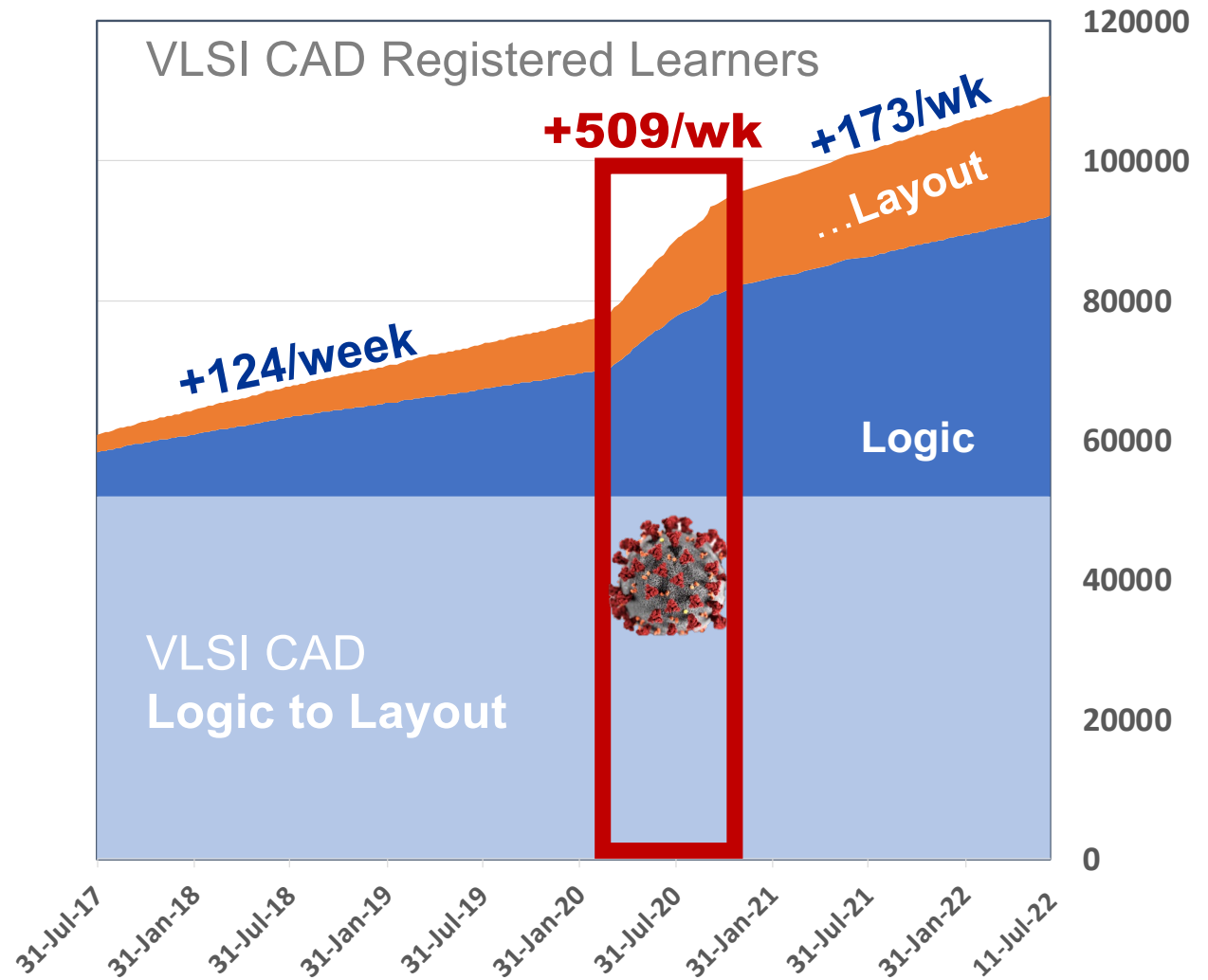
Enrollment: Coursera CAD MOOCS



Enrollment: Coursera CAD MOOCs



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Thanks!

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