



Rob A. Rutenbar

2017 ESDA/CEDA Phil Kaufman Award

Award Presenter:

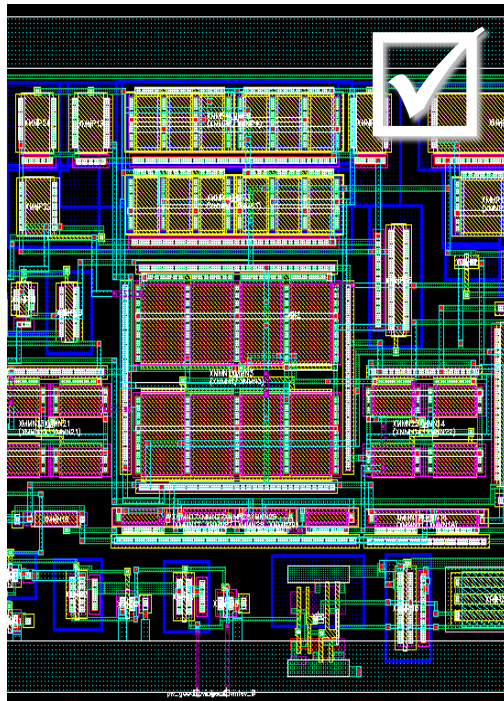
Martin D.F. Wong

Univ. of Illinois at Urbana-Champaign

An Appreciation, in Three Acts ...



The ideas



The impact

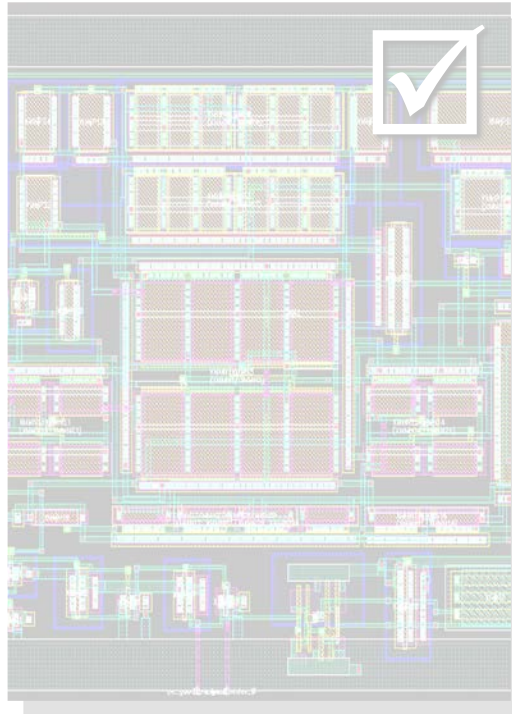


The individual

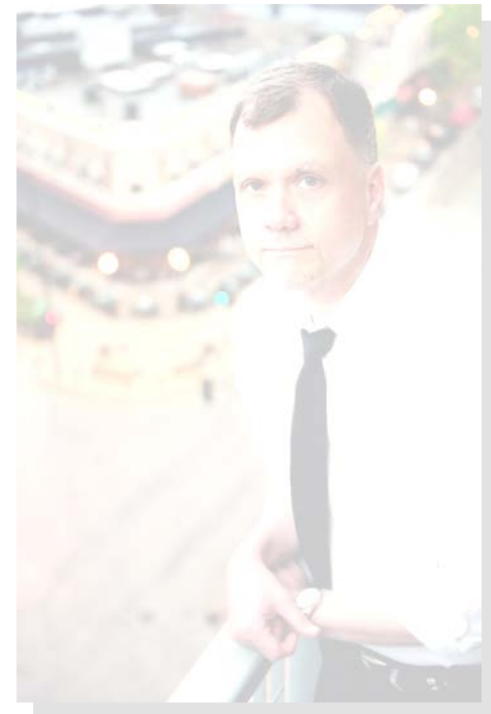
An Appreciation, in Three Acts ...



The ideas



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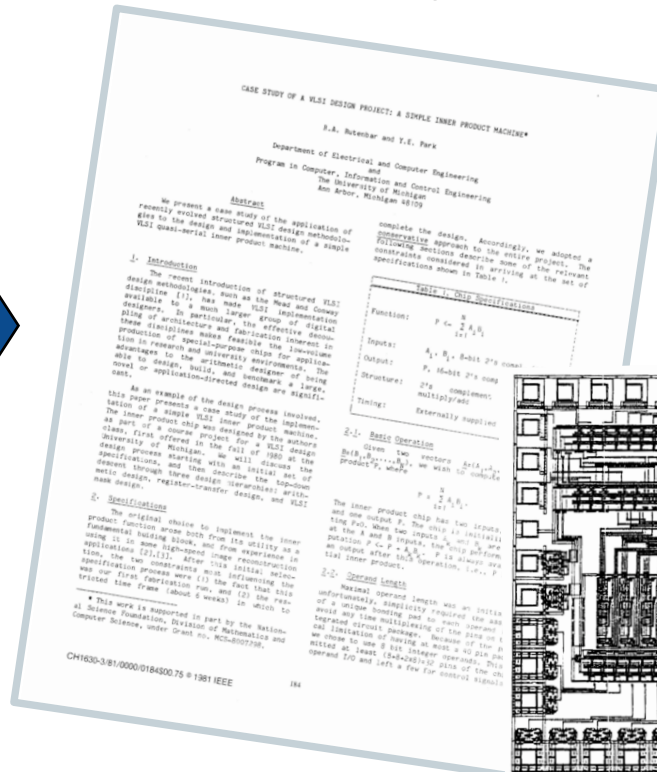
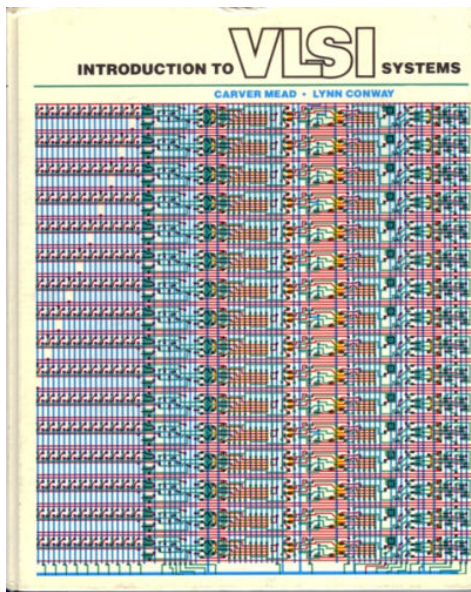


The individual

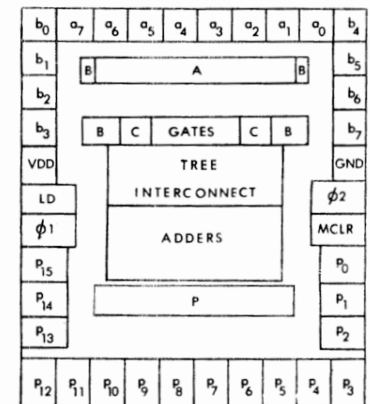
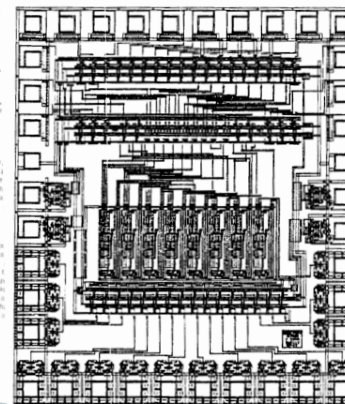
Some History: In the 1980s...



- It became possible for students & faculty to **do chips**
- This was the VLSI revolution, and **Rob was there**



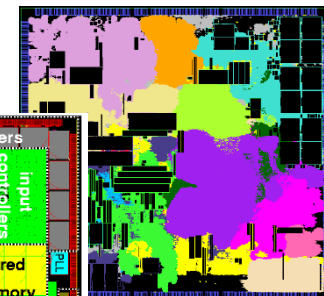
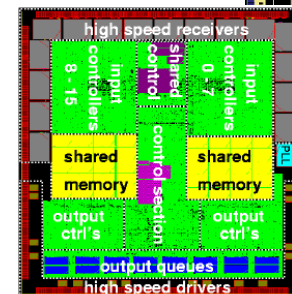
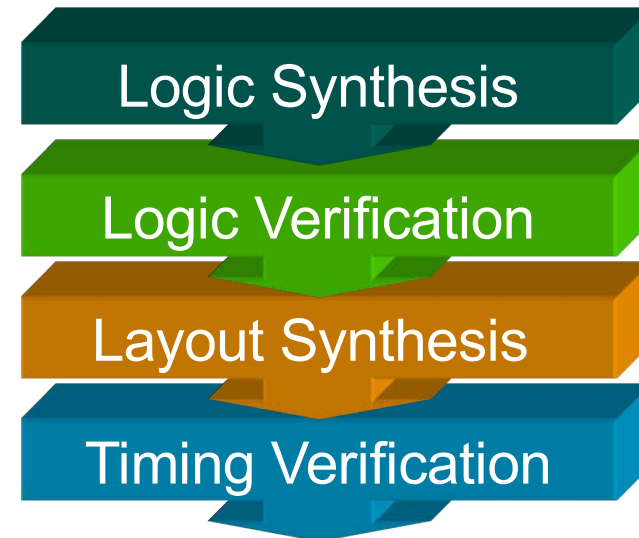
Process: 4um NMOS
Size: 4.4x5.1 mm
Complexity: 503 devices
Function: $A += B * C$



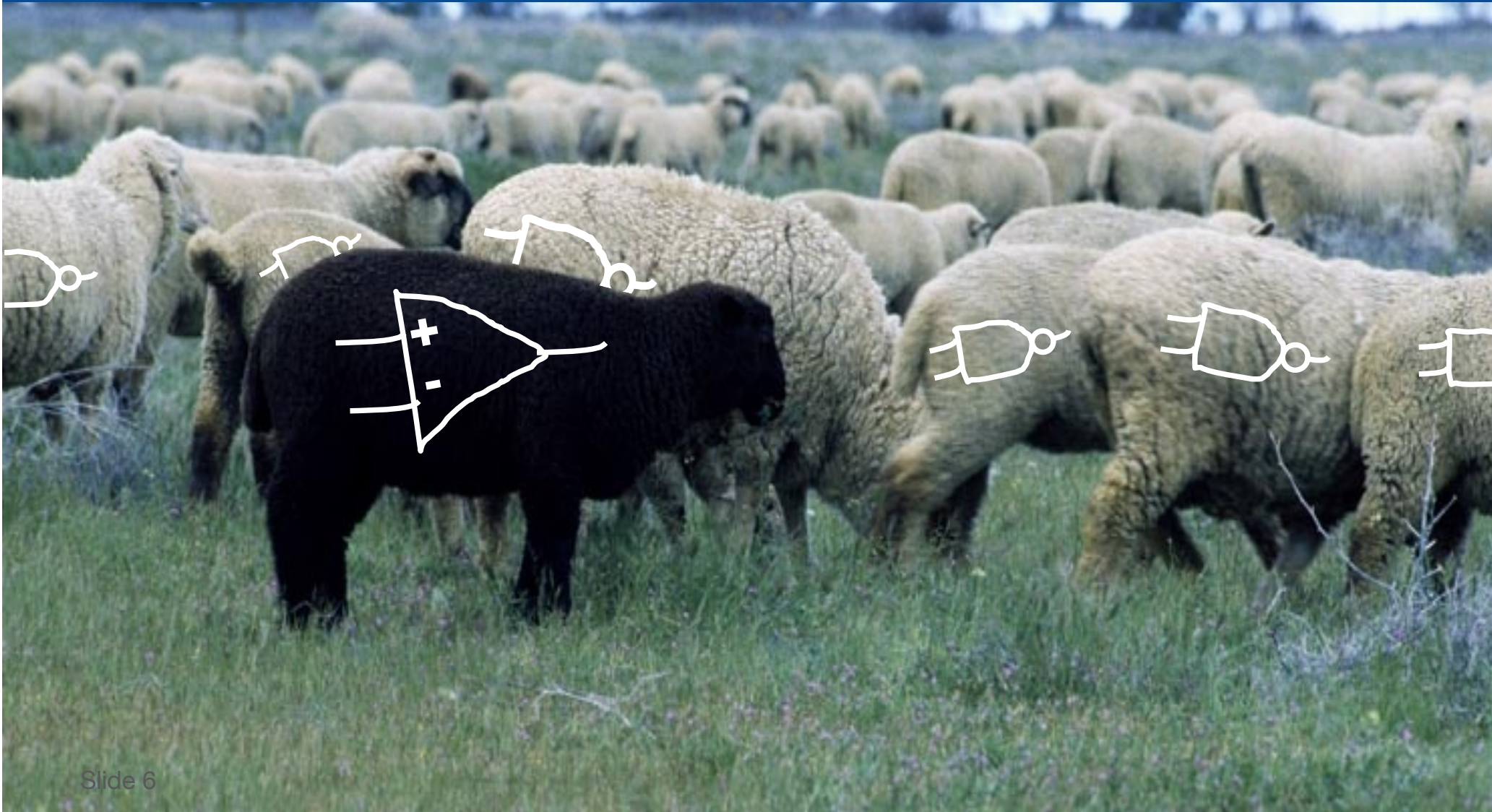
80s and 90s → Digital ASIC Flows



- Big ideas in **synthesis**
- Big ideas in **verification**
- Big ideas in **logic**
- Big ideas in **layout**
- Big ideas in **timing**
- And flows, flows, **FLAWS**...



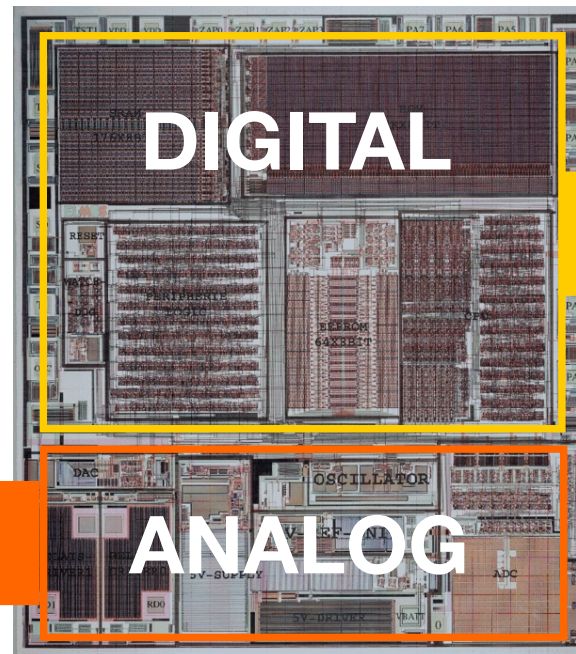
Just One Little Problem...



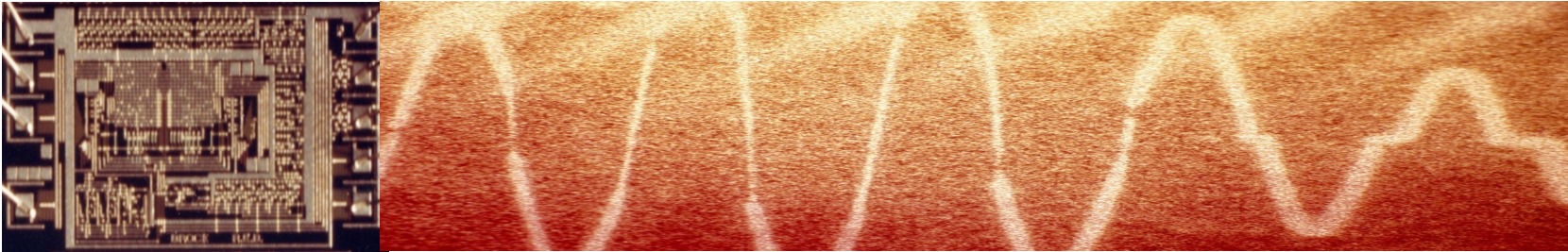
Analog CAD Was Not Happening



- Aside from core simulation tech (SPICE-ish), EDA was a vast, empty wasteland for **non-digital designs**



Some Kaufman-Centric History...



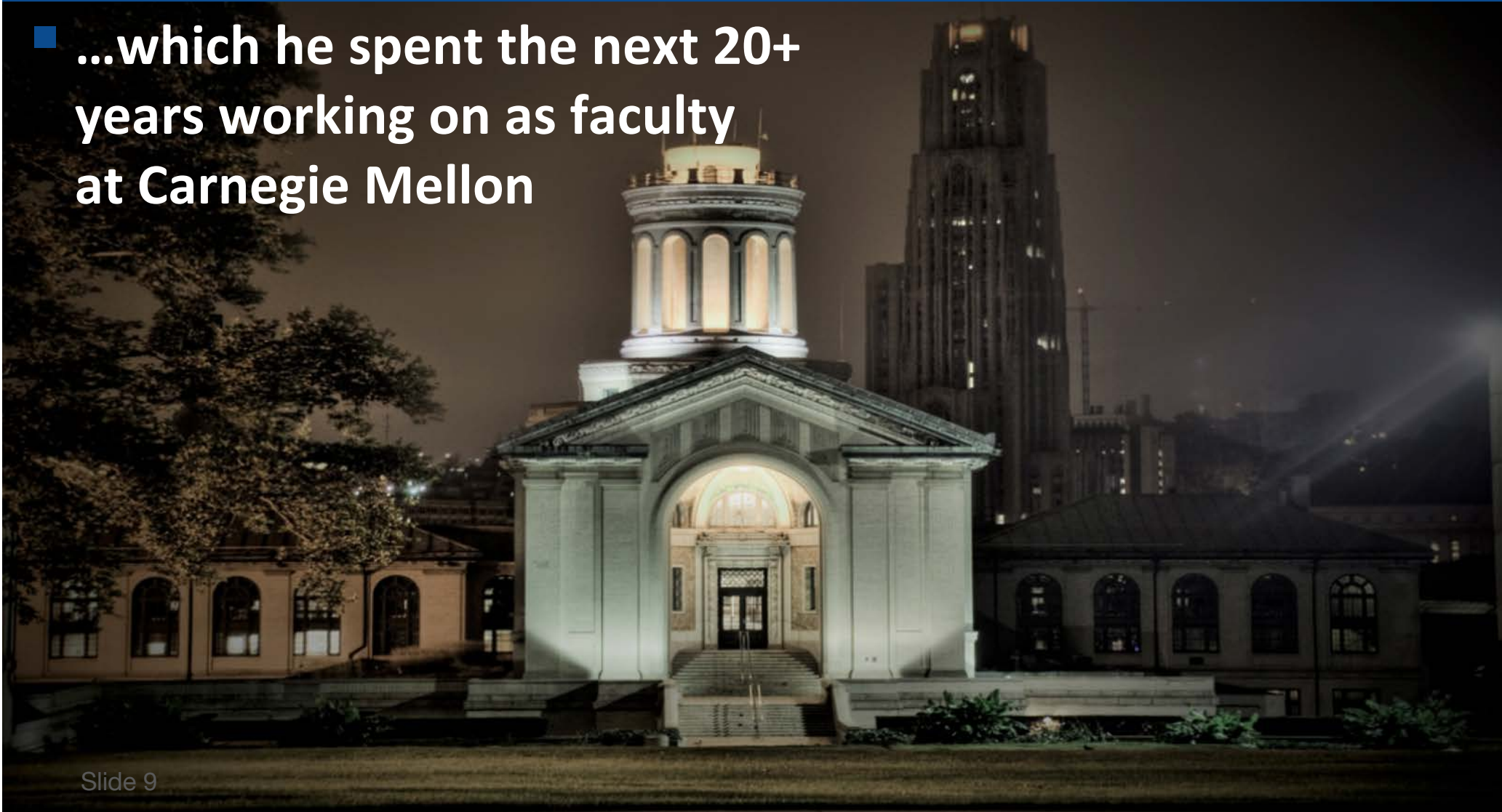
- **A strong tradition of awards to those simulation pioneers**



But Rob Saw a Large Opportunity



- ...which he spent the next 20+ years working on as faculty at Carnegie Mellon



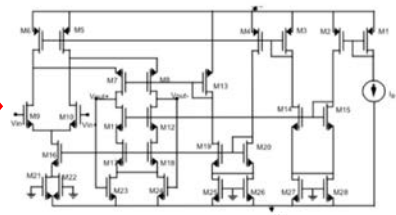
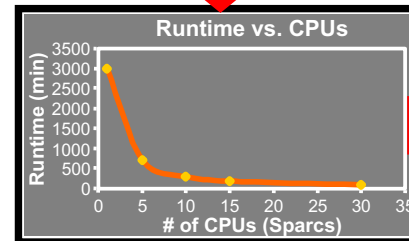
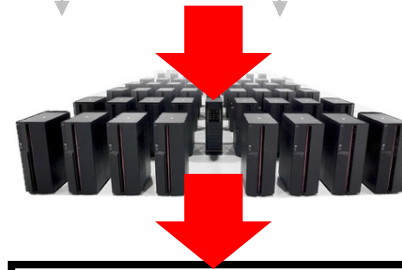
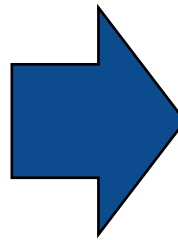
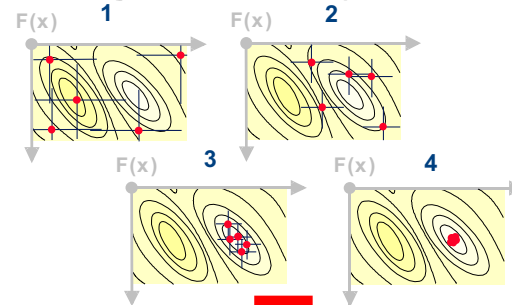
Rob's Big Idea



- Analog – it's *art*, it's *deep*, *mysterious*, *painful*, *sublime*...



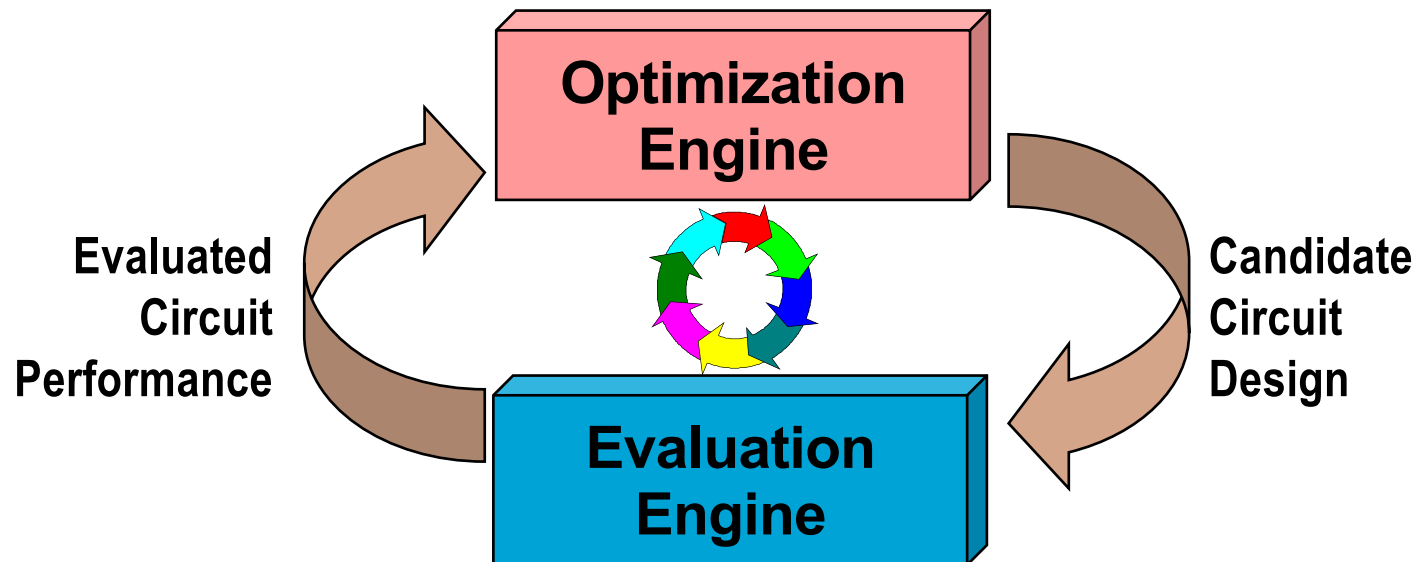
- NO – it's *optimization*. Big hard optimization.



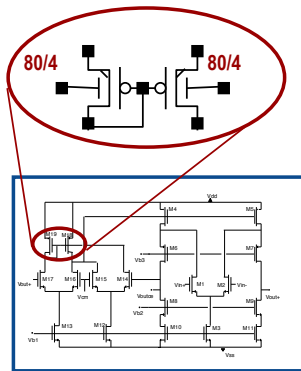
Rob's Big Idea, Revisited



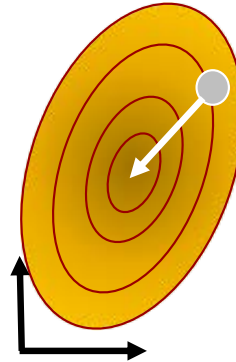
- Clever models & engines can support *principled search* for best analog design to *meet designer constraints*



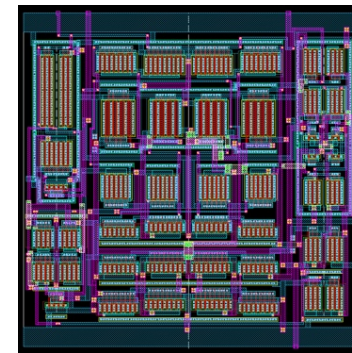
Pursued Across Breadth of Analog



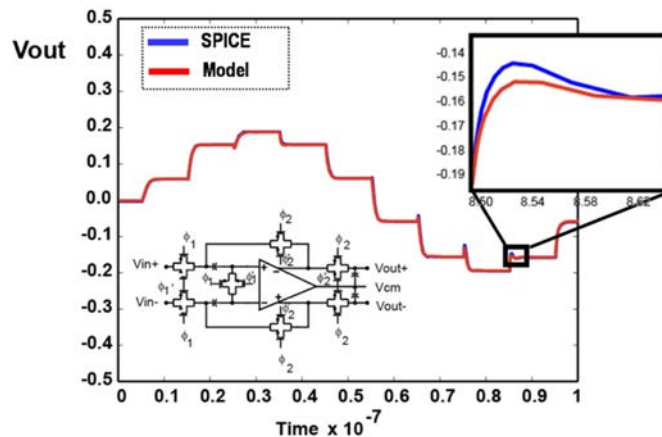
SIZING



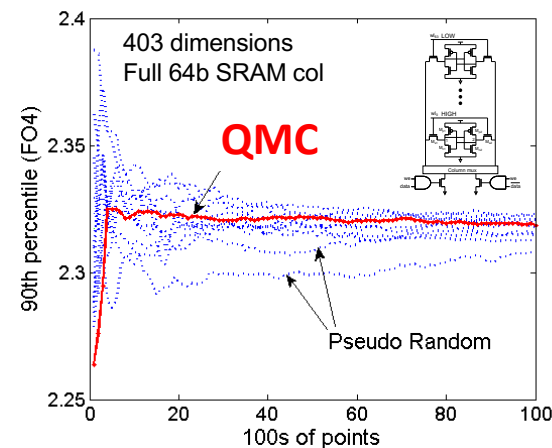
OPTIMIZATION



LAYOUT



MACROMODELING



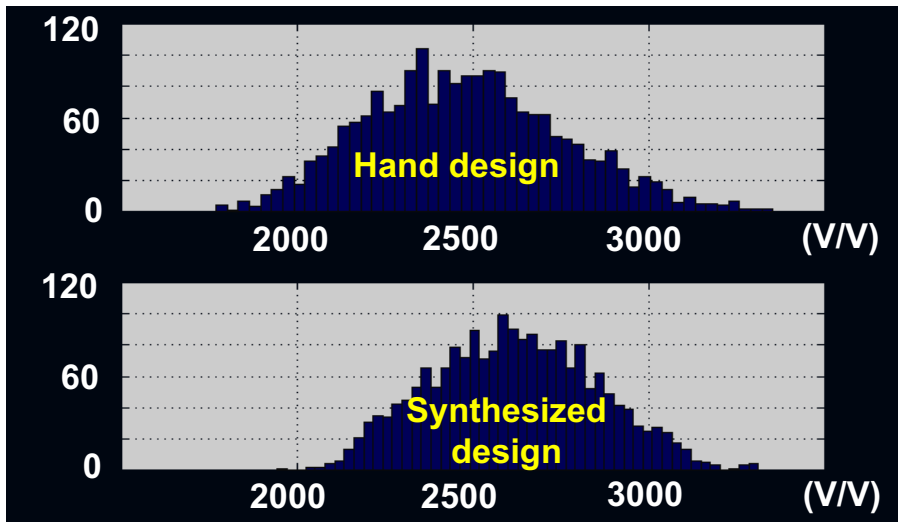
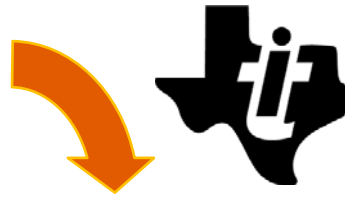
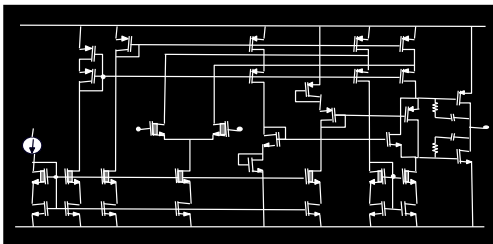
STATISTICS



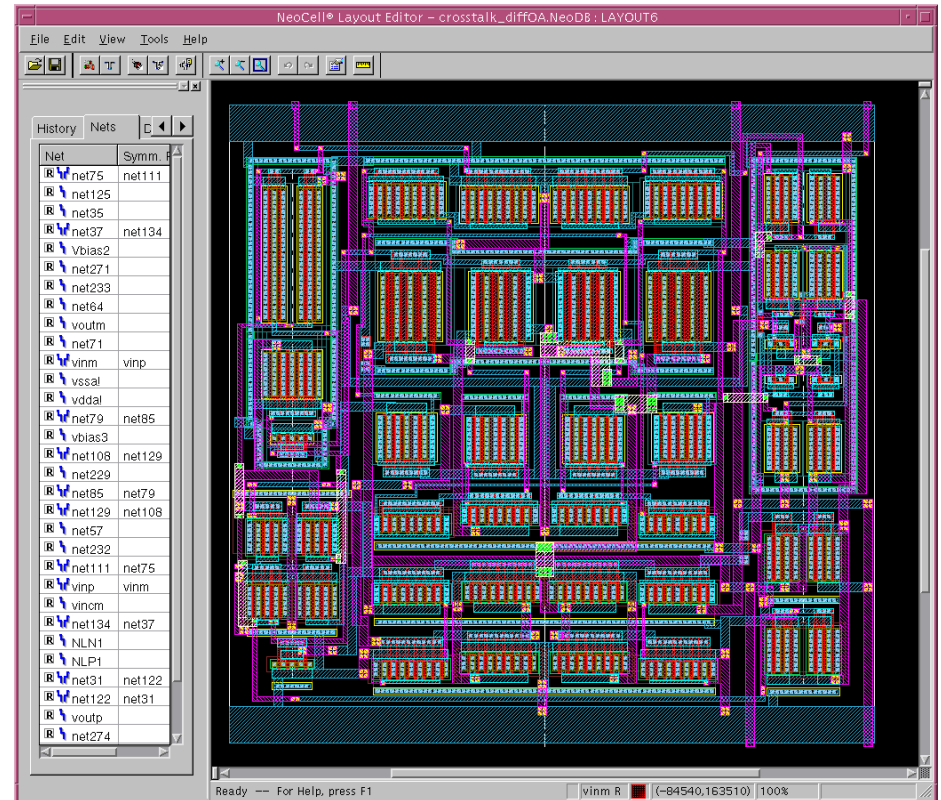
Two Analog Examples



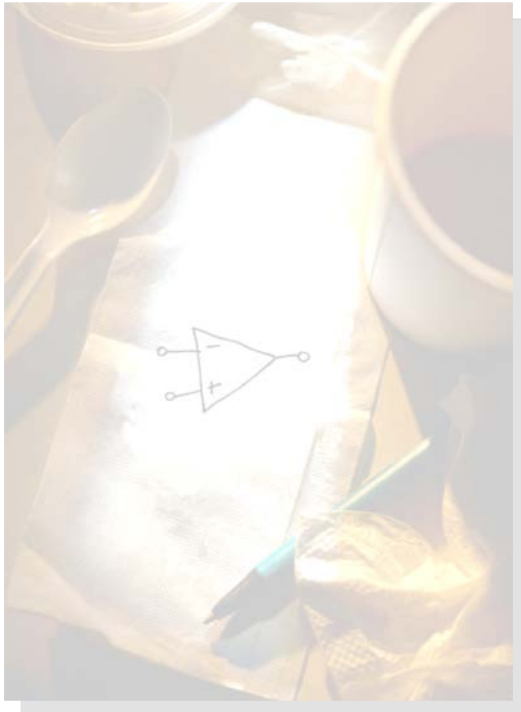
- Practical Spice-in-the-Loop optimizers that “just work”



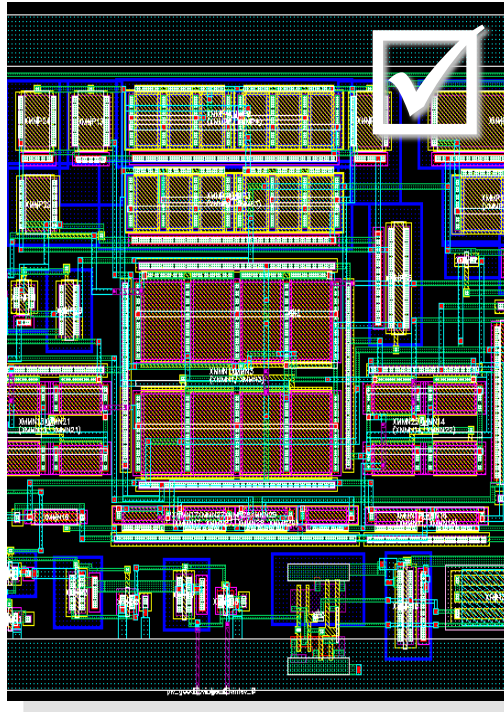
- Automatic layouts with **manual aesthetics & performance**



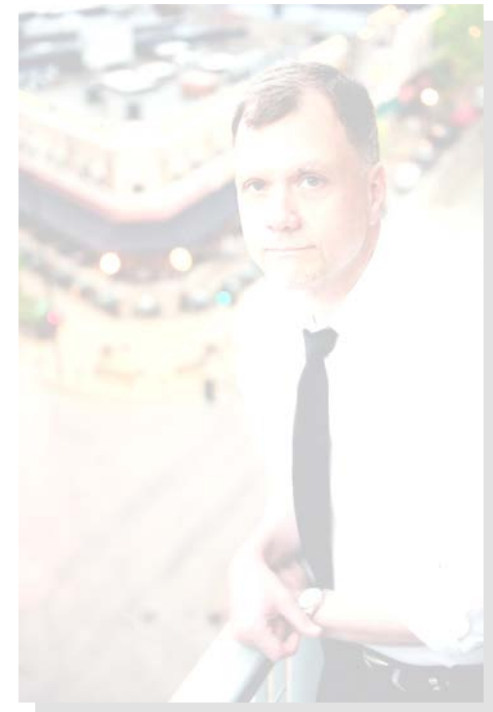
An Appreciation, in Three Acts ...



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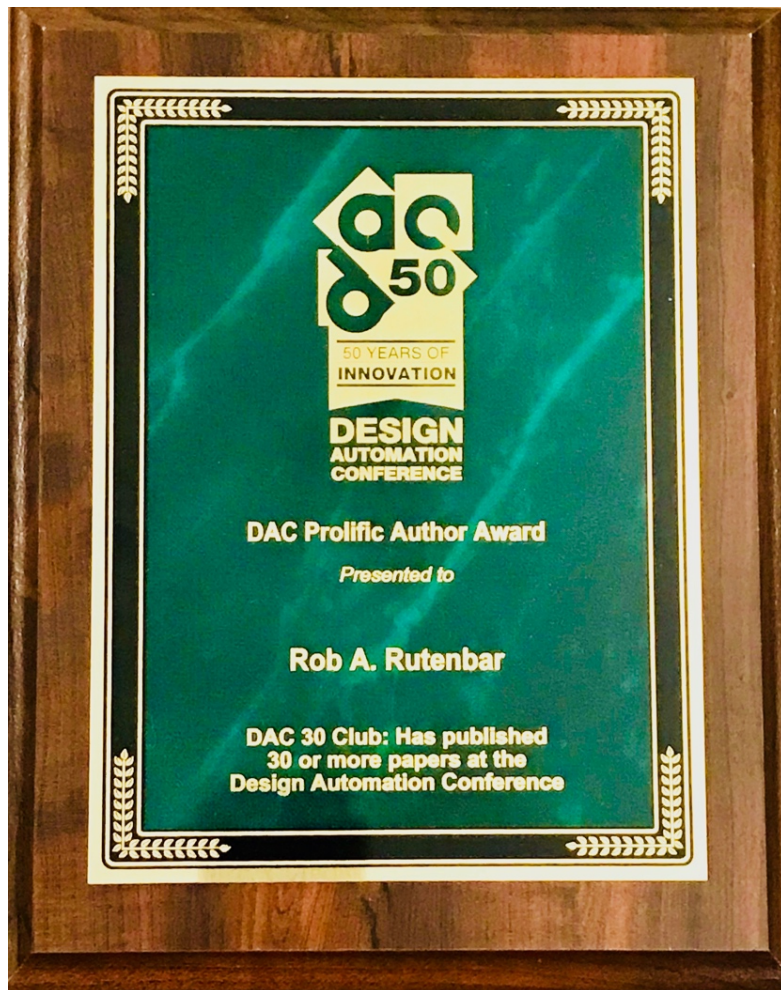


The impact



The individual

Academic Impact (Of Course)



- **200+** papers, books etc
- **~10,000** citations
- **Many, many awards**
 - **3** DAC Best Papers
 - **2** IEEE TCAD Pedersen Awards
 - **1** DATE Best Paper
 - **1** ICVLSI Best Paper

Rob Really "Wrote the Books" Here



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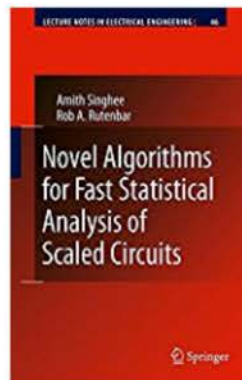
Textbooks

Textbook Rentals

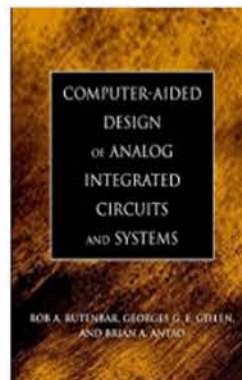
Sell Us Your Books

Best Books of the Month

Rob A. Rutenbar



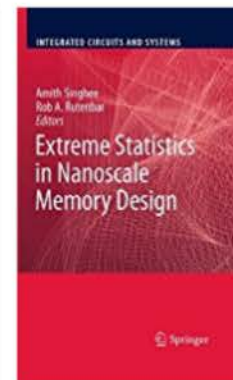
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Hardcover



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Hardcover



\$197.92
Paperback



\$150.01
Hardcover



\$17.00
Hardcover



\$417.81
Paperback

Books by Rob A. Rutenbar

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Contributed to EDA & Tech Community



EE Times Connecting the Global Electronics Community

SIGNALS

Synthesis proves to be Holy Grail for analog EDA

Analog synthesis—the ability to connect efficient analog circuits from top-level descriptions—has become the holy grail of analog EDA development. But the researchers making the progress in synthesis are for the most part working in isolation. They are largely unaware of progress being made in other parts of the world, and vice versa.

Significant progress appears to be coming from the work of three professors and students: Bob Brunton and Richard Carley at Carnegie Mellon University (Pittsburgh), Ranga Varma at the University of Cincinnati, and George Golea at the Catholic University of Leuven (Belgium).

“One of the biggest problems in analog synthesis is the use of nonparametric simulation models. It is difficult to get designers to use the idea that synthesis generally works,” he said. *EE Times* manufacturers are making and selling digital circuits have large investments in models and simulators, as well as qualifications and capabilities. They are not looking to abandon Verilog or

Carnegie Mellon has gotten as many as 24 universities to operate in parallel, and Brunton has the best topology for a power amplifier circuit. For example, with 200 MHz, the maximum is up to 30 GHz, or an equivalent of 20 GHz. The system for each circuit is used as one a half.

lution accuracy for speed, in reducing design-to-synthesis. “For systems on-chip designs, that doesn’t work,” Brunton said. He noted that the Marletta and Ananda tools will build accurate top-ups, making references and other analog building blocks, though not complex signal modulation or phase-locked loops. But Brunton is confident that the ability to synthesize these building blocks will give rise to the ability to build larger systems.

Meanwhile, researchers at the Laboratory for Digital Design Environments at the University of Cincinnati have developed a “nonlinear neural” algorithm that automates an exhaustive search for alternative circuit topologies to synthesis. De-

George Golea’s Bob Brunton plans to perform a neural circuit synthesis by utilizing a “top-down” to bottom-up. Both other development are designed to build any system to step and other analog building blocks, opening the door to larger circuits.

signs are named as VLSI (VERY-LARGE-SCALE INTEGRATION) Environments, the synthesis process produces a number of circuit components that represent various sizes and performance capabilities. Brunton researcher John



INSIDE THIS ISSUE: TECHNOLOGY QUARTERLY

The Economist

America and its immigrants
Dealing with Iran
In praise of the odd SKT
Can the new boss revive Sony?

The real digital divide

The talking cure
Speech technology: Good speech recognition requires a fast PC. A chip-based implementation could make the technology more portable.


Speech recognition will never be a household name until it can be used on a mobile phone. A new chip might provide the opportunity. It is being created by a team of researchers from Carnegie Mellon University and the University of California at Berkeley to do one thing, and one thing only: speech recognition. Using a new, non-linear based approach to the problem, the researchers hope to create a chip that performs speech recognition much more efficiently than is currently possible using software-based recognition systems. If they are right, it might soon become possible to dictate an e-mail to your BlackBerry, or edit your mobile phone's address book using voice commands alone.

Speech recognition software has been on the market for over a decade, and in the past five years it has become almost essential for many people. But it is not perfect. For some users at least, it is frustratingly slow and often fails to understand what you say. It is also expensive. The new chip, developed by Carnegie Mellon and UC Berkeley, is a portable device to do the same kind of recognition, but it is much faster, and in many cases, it is much cheaper. Why would a chip-based solution be any better?


The answer is simple: doing something as well as it can be done, but doing it better.

Speech recognition is a complex task. It involves understanding the human voice, which is a complex signal. It is a task that is difficult to do with software. The new chip, however, is designed to do this task much more efficiently. It is a task that is difficult to do with software, but it is a task that is easy to do with a chip.


THURSDAY SKY TALKS



Paul Kocher
Cryptography Research, Inc.
11:30am – Room 309



Sudip Dosanjh
Lawrence Berkeley National Lab
2:30pm – Room 306

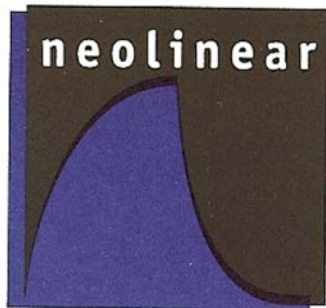


Rob A. Rutenbar
Univ. of Illinois at Urbana-Champaign
5:00pm – Room 306



DESIGN AUTOMATION CONFERENCE

More Critically – Deep Industry Impact



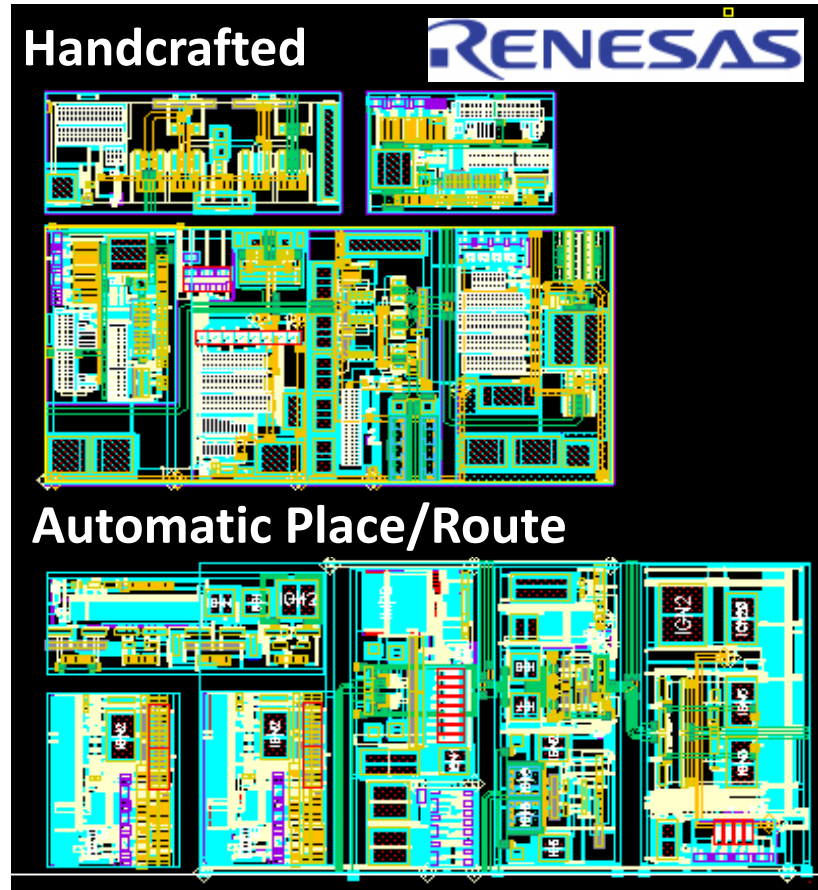
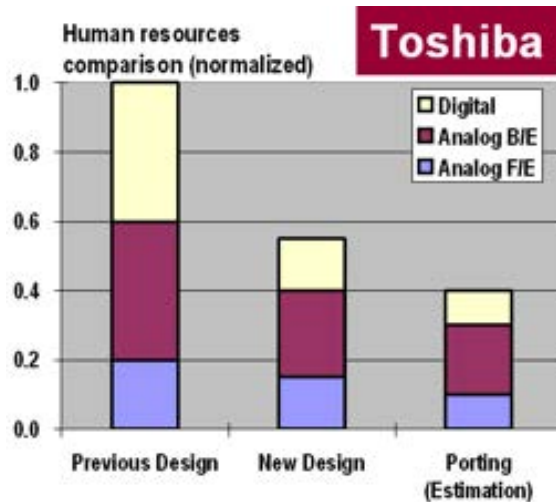
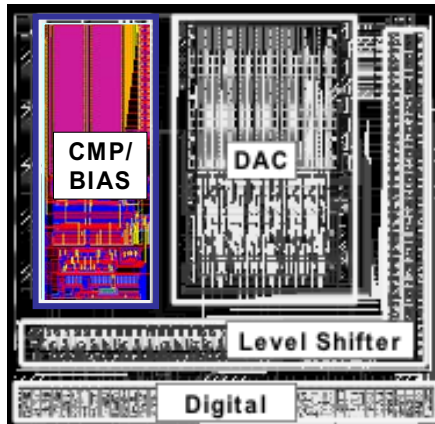
Rob A. Rutenbar
Chief Technologist

Neo Linear, Inc.
311 South Craig Street
Suite 102
Pittsburgh, PA 15213
Tel 412.681.1080
FAX 412.681.0802

rutenbar@neoliner.com



Neolinear: Front-to-Back Analog Tools



Neolinear: Customers



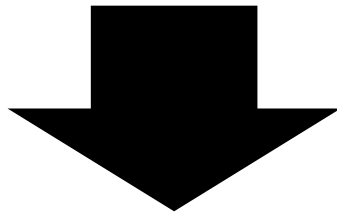
NeoCircuit & NeoCircuit-RF



NeoCell



2004: Neolinear → Cadence



cādence™

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Financial News

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Press Release

Source: Cadence Design Systems, Inc.

Cadence to Acquire Neolinear

Tuesday April 6, 8:30 am ET

Neolinear Technology to Accelerate Design Cycle and Enhance Silicon Yield

SAN JOSE, Calif.--(BUSINESS WIRE)--April 6, 2004--Cadence Design Systems, Inc. (NYSE:[CDN](#) - [News](#)) today announced it plans to acquire Neolinear, Inc., a privately held company. Neolinear's rapid analog design technology is critical for the consumer and communications markets where semiconductors are increasingly differentiated by their analog content. The Neolinear team will bring additional strong A/MS and RF expertise into Cadence and play a key role in driving ongoing innovations for improving yield and speeding IP reuse in the Cadence® Virtuoso® custom design platform. Neolinear's NeoCircuit and NeoCell are already an extended part of the industry-leading Virtuoso platform through an OEM agreement between the two companies.

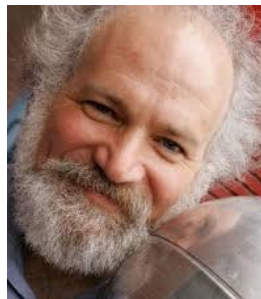
Now: Cadence Pittsburgh



But Also Another Impact: Teaching



- Rob is an extraordinary, dedicated **teacher**
- His CMU class alums are a **Who's-Who of EDA leaders**

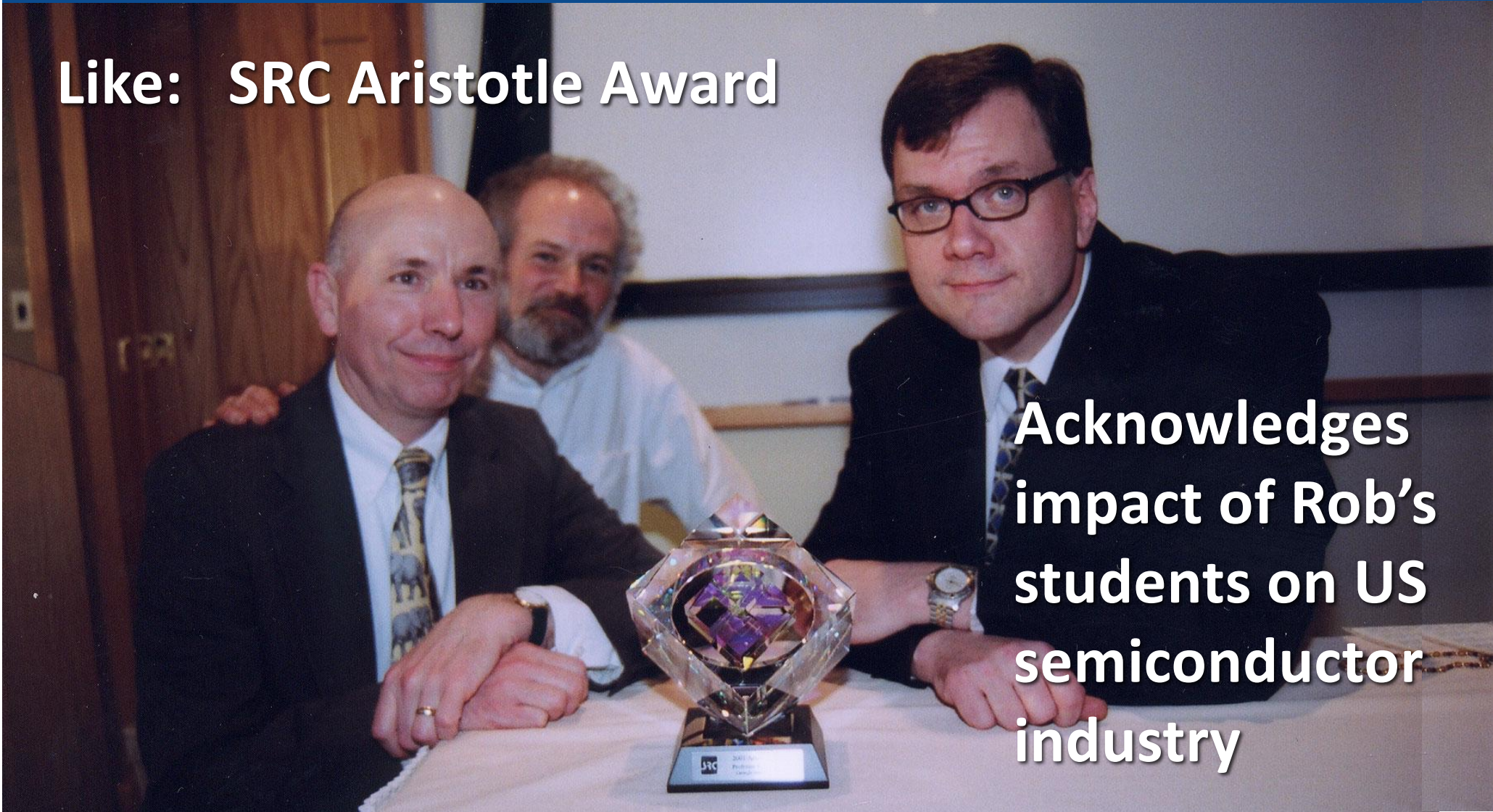


Won Major Teaching Awards



Like: SRC Aristotle Award

**Acknowledges
impact of Rob's
students on US
semiconductor
industry**



Another Measure of Impact



- What happens when you type this...?

Google

VLSI CAD



All

Images

Videos

News

Maps

Settings

Tools

Answer: You Get Rob (8 of Top 10!)



About 341,000 results (0.39 seconds)

#1 Rob's MOOC

VLSI CAD Part I: Logic | Coursera

<https://www.coursera.org/learn/vlsi-cad-logic>

About this course: A modern VLSI chip has a zillion parts -- logic, control, memory , interconnect, etc. How do we design these complex chips? Answer: CAD software tools. Learn how to build theseA modern VLSI chip is a remarkably complex beast: billions of transistors, millions of logic gates deployed for computation and ...

#2 Rob's MOOC

VLSI CAD Part II: Layout | Coursera

<https://www.coursera.org/learn/vlsi-cad-layout>

About this course: You should complete the VLSI CAD Part I: Logic course before beginning this course. A modern VLSI chip is a remarkably complex beast: billions of transistors, millions of logic gates deployed for computation and control , big blocks of memory, embedded blocks of pre-designed functions designed by third ...

#3 Bootleg of Rob's MOOC

VLSI CAD: Logic to Layout Lecture 001 Welcome and Introduction ...



<https://www.youtube.com/watch?v=WLdbujc-aH4>

Mar 11, 2013 - Uploaded by Alireza Saberi

Alireza Saberi. ... Course is presented by professor Rob A. Rutenbar is the Abel Bliss Professor and ...

#4 Review of Rob's MOOC

Reviews for VLSI CAD Part I: Logic from Coursera | Class Central

<https://www.class-central.com> Coursera

★★★★★ Rating: 5 - 3 reviews

A modern VLSI chip has a zillion parts -- logic, control, memory, interconnect, etc. How do we design these complex chips? Answer: CAD software tools. Learn how to build theseA modern VLSI chip is a remarkably complex beast: billions of transistors, millions of logic gates deployed for computation and control, big blocks of ...

Reminder: Massive Open Online Courses



Internet-scale video
(for instruction)



Cloud-based assignments
(for eval & grading)



Super Cheap

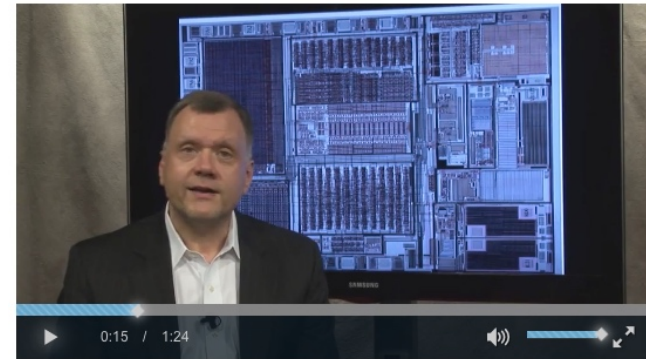


MOOCs

In 2013, Rob Launched First EDA MOOC



- And, its been running ever since, including **right now...**



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Courses Partners About | Sign In Sign Up

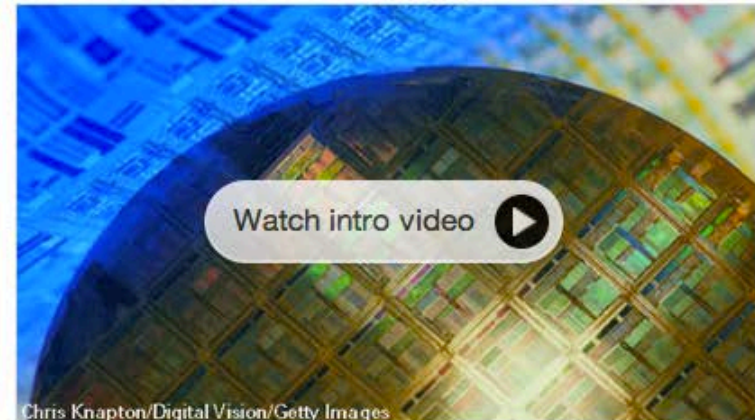
ILLINOIS

VLSI CAD: Logic to Layout

Rob A. Rutenbar

A modern VLSI chip has a zillion parts -- logic, control, memory, interconnect, etc. How do we design these complex chips? Answer: CAD software tools. Learn how to build these tools in this class.

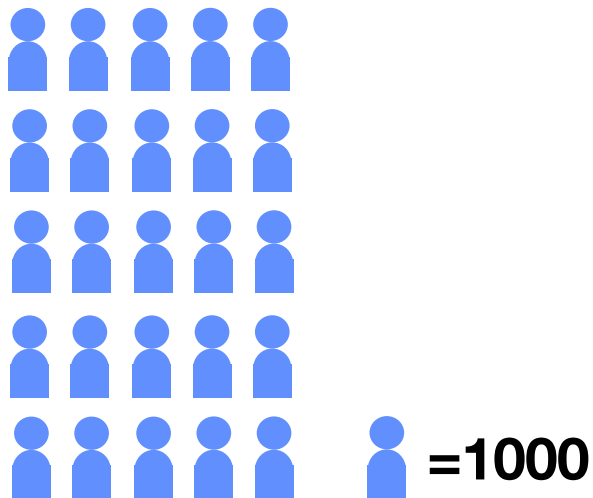
Workload: 10-12 hours/week



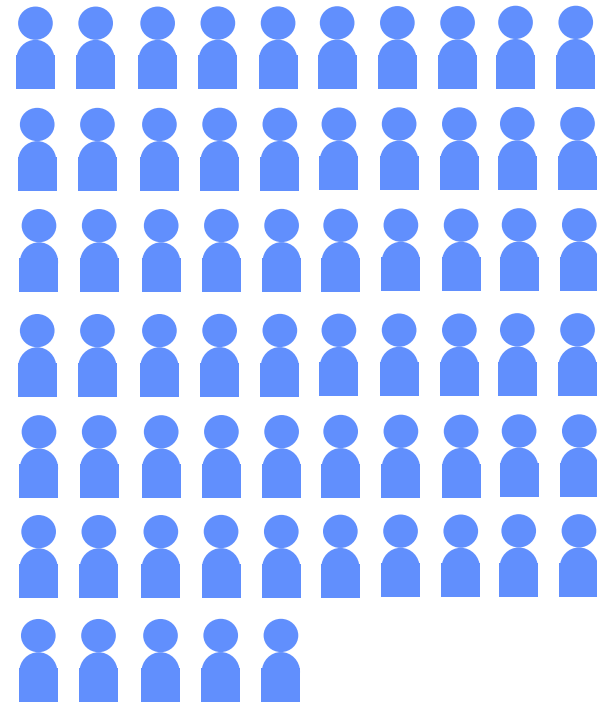
EDA MOOC Impact



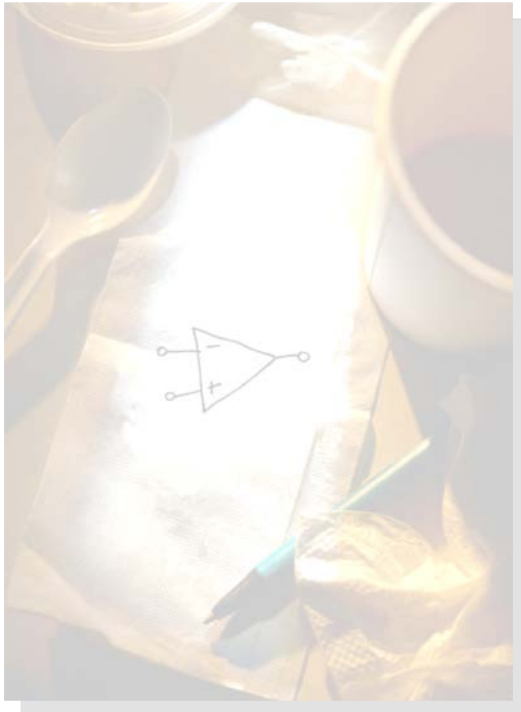
- It is estimated there are roughly **25,000** EDA professionals on the planet



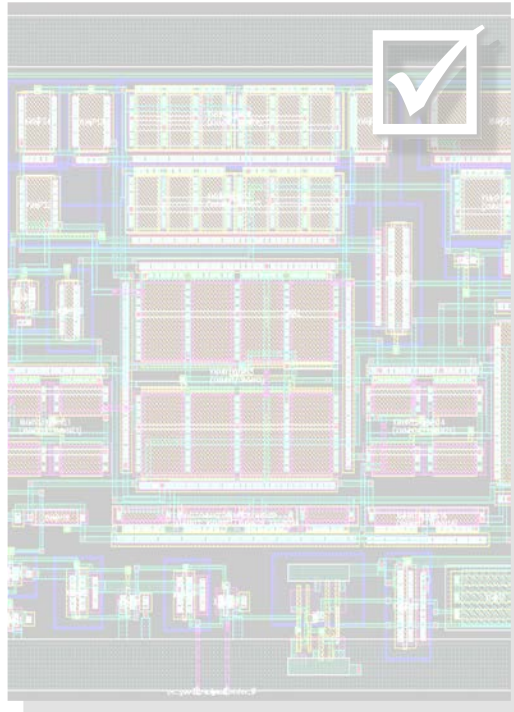
- Rob's MOOCs, since 2013, have enrolled **64,310** of them (**~100 more every week**)



An Appreciation, in Three Acts ...



The ideas

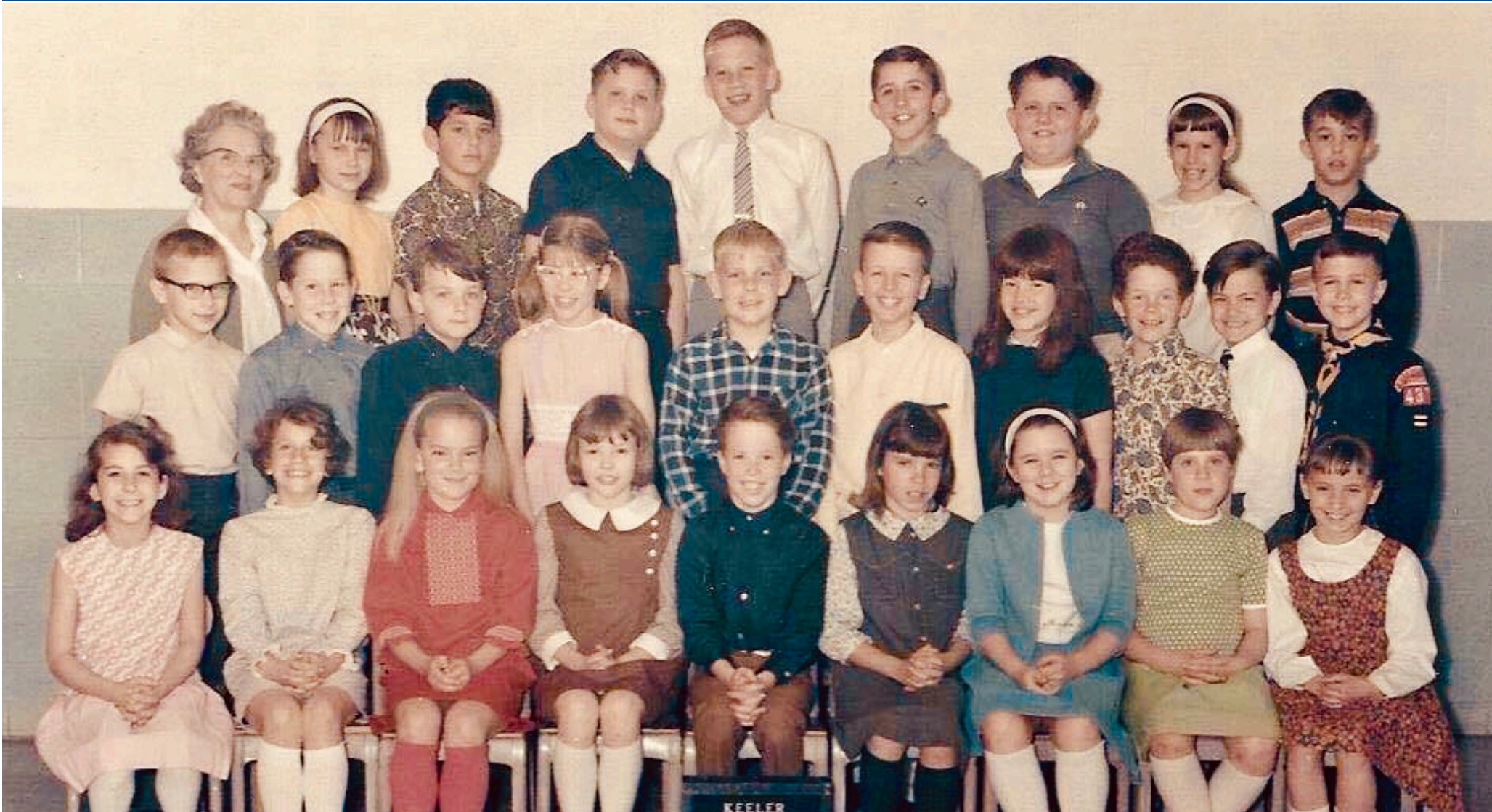


The impact



The individual

Just Another Kid from Detroit...



Rob: Five Schools, Forty Years



'75-'78 Wayne (BS)

**WAYNE STATE
UNIVERSITY**



'78-'84 Michigan (MS, PhD)

M UNIVERSITY OF MICHIGAN



'84-'09 CMU (Faculty)

**Carnegie
Mellon
University**



'10-'17 UIUC (Head)

I ILLINOIS



'17-now Pitt (VC Research)



**University of
Pittsburgh**

Prof. Rutenbar → Manager/Boss



- **Head of CS at University of Illinois at Urbana-Champaign**



- **Vice Chancellor for Research at University of Pittsburgh**



New Friends, New Challenges



Rob's Key Nontechnical Achievements



Slide 35

Rob Rutenbar: 2017 Kaufman Award



**Congratulations to Rob,
our friend & colleague,
for his lifetime of
contributions to EDA**

