Rob A. Rutenbar

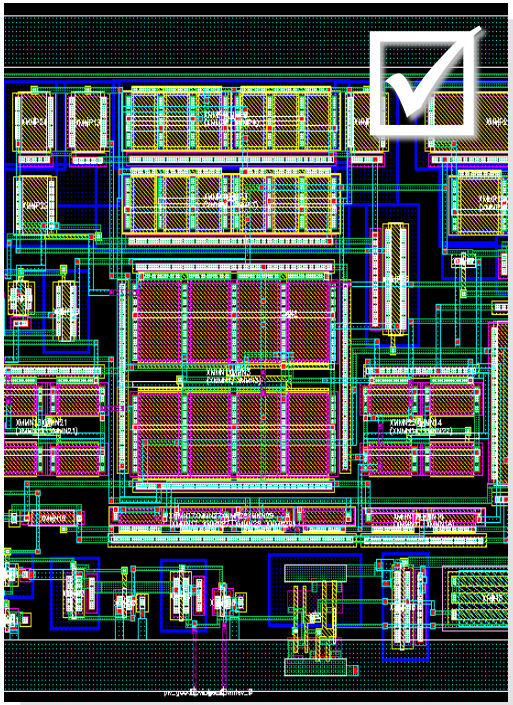
2017 ESDA/CEDA Phil Kaufman Award

Award Presenter:

Martin D.F. Wong
Univ. of Illinois at Urbana-Champaign

An Appreciation, in Three Acts …

The ideas

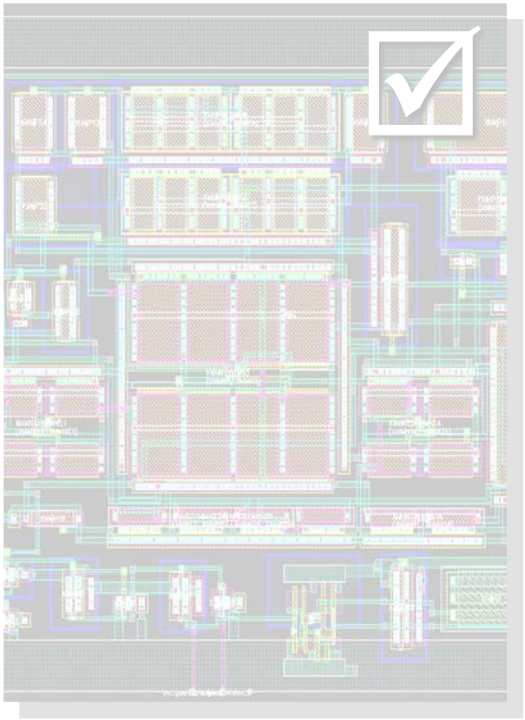


The impact

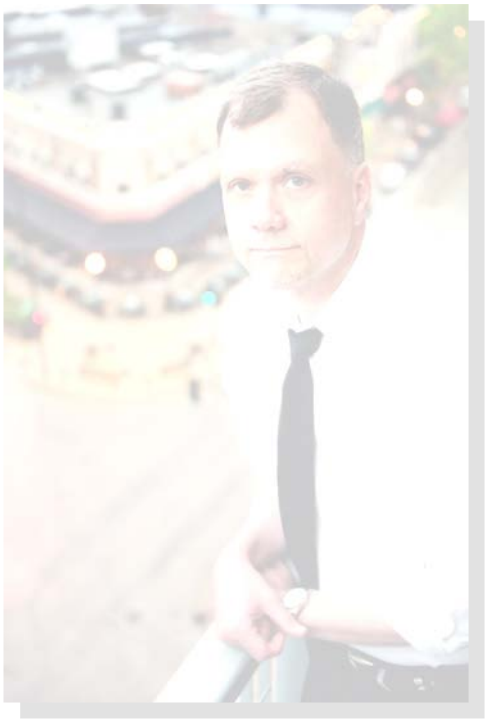
The individual

An Appreciation, in Three Acts …

The ideas



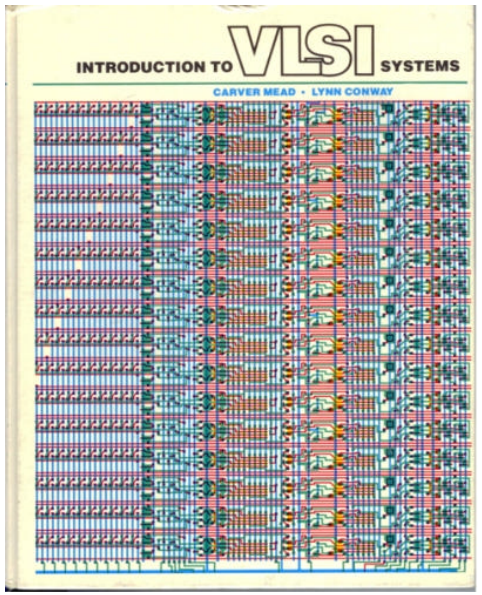
The impact

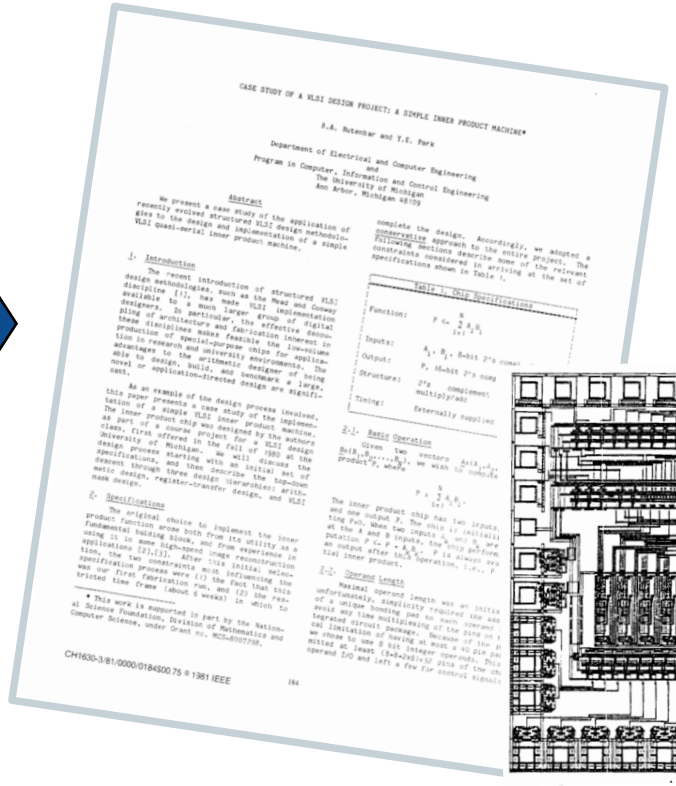


The individual

Some History: In the 1980s…

- **It became possible for students & faculty to do chips**
- **This was the VLSI revolution, and Rob was there**




CASE STUDY OF A VLSI DESIGN PROJECT: A SIMPLE INNER PRODUCT MACHINE*

R.A. Rutenbar and Y.E. Park

Department of Electrical and Computer Engineering
and
Program in Computer, Information and Control Engineering
The University of Michigan
Ann Arbor, Michigan 48109

Abstract

1. Introduction

2. Specifications

2-1. Basic Operation

2-2. Operand Length

* This work is supported in part by the National Science Foundation, Division of Mathematics and Computer Science, under Grant no. MCS-8007708.

CH1630-3/81/0000/0184$00.75 © 1981 IEEE

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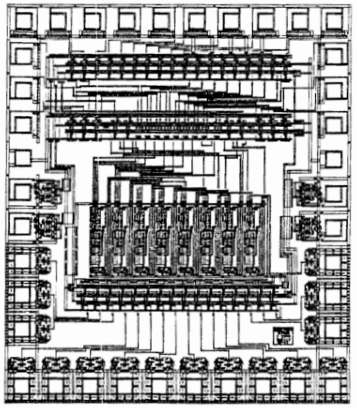
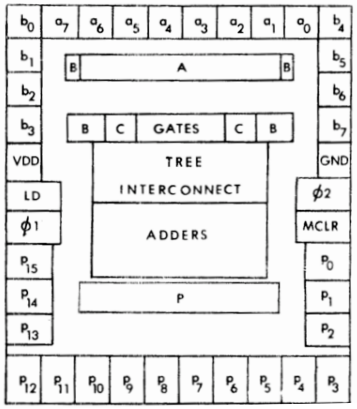
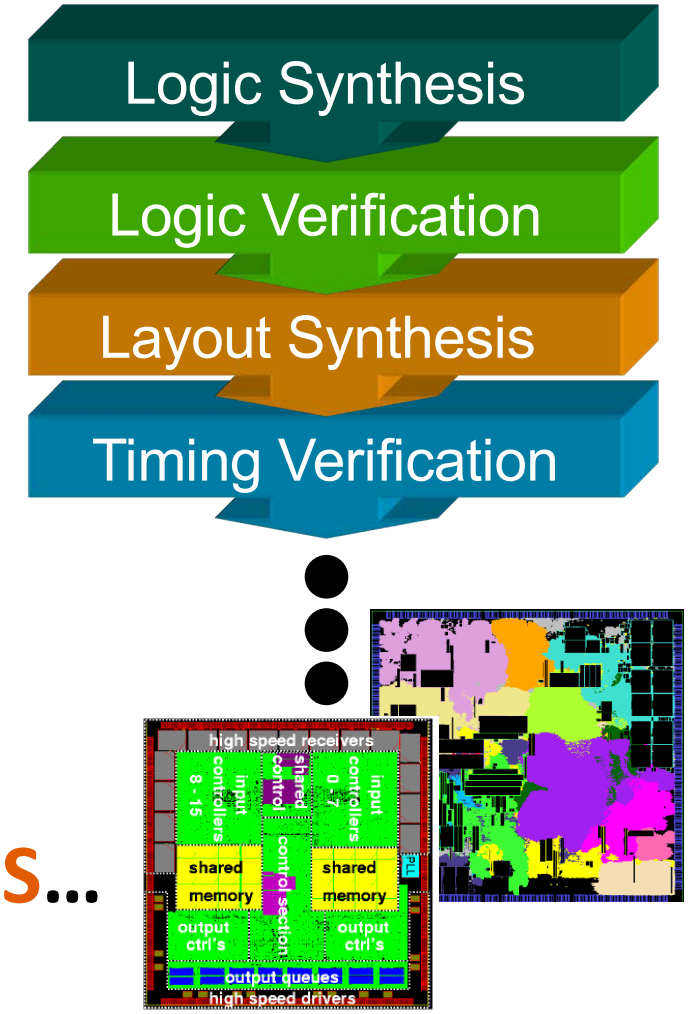
Process: 4um NMOS
Size: 4.4x5.1 mm
Complexity: 503 devices
Function: A += B*C



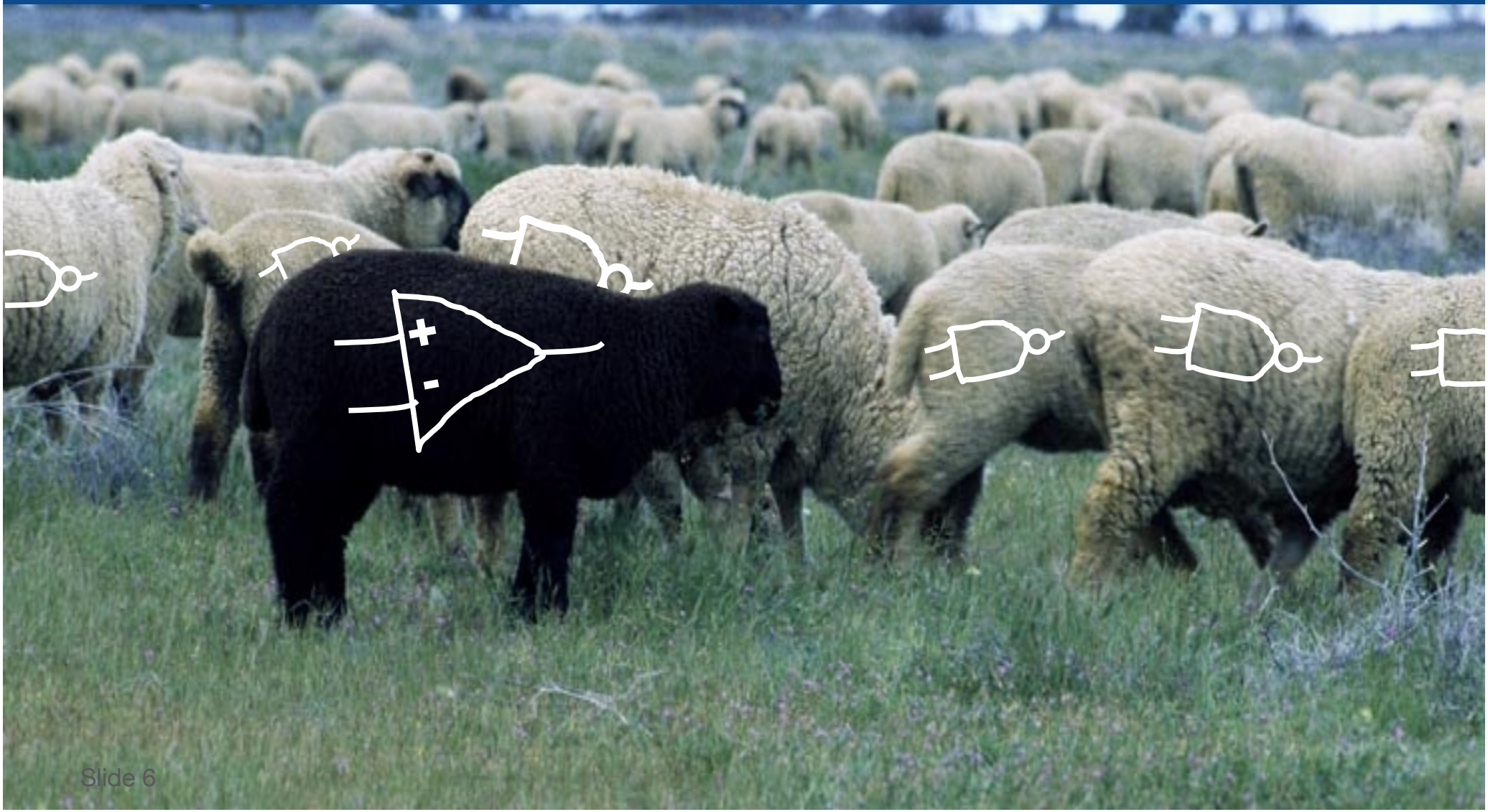


80s and 90s → Digital ASIC Flows

- Big ideas in **synthesis**
- Big ideas in **verification**
- Big ideas in **logic**
- Big ideas in **layout**
- Big ideas in **timing**
- And flows, flows, **FLOWS**…

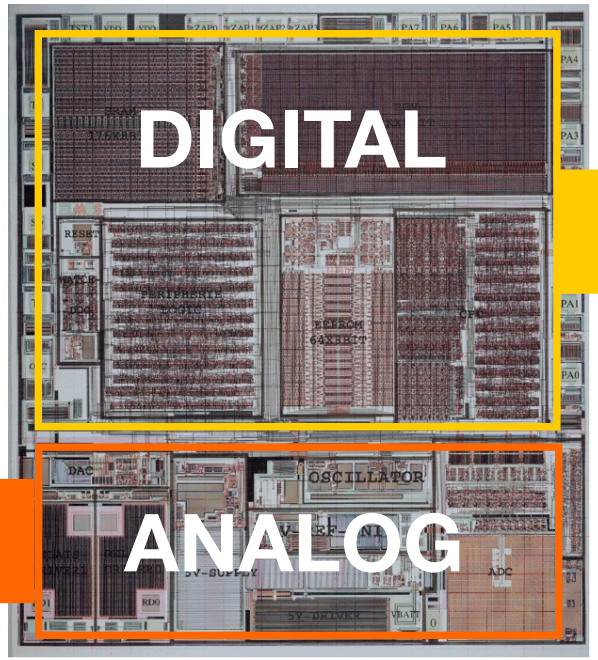


Just One Little Problem…

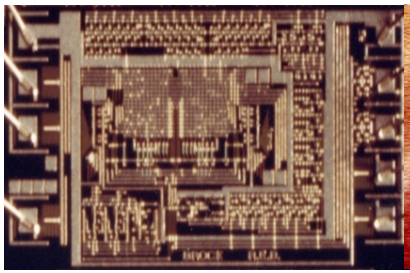


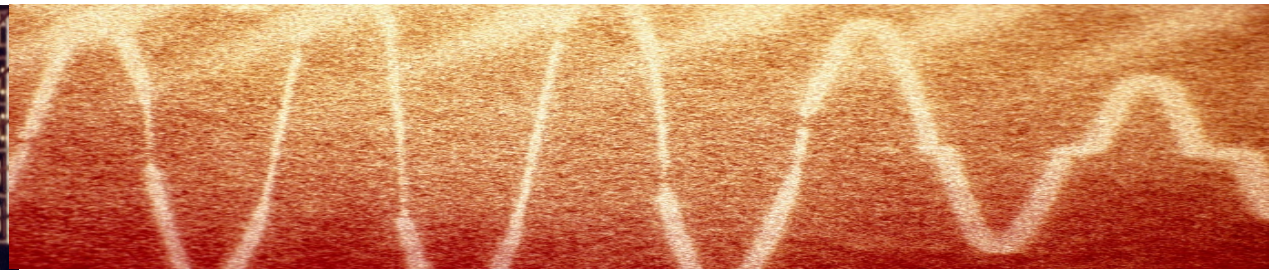
Analog CAD Was Not Happening

- **Aside from core simulation tech (SPICE-ish), EDA was a vast, empty wasteland for non-digital designs**



Some Kaufman-Centric History…





- **A strong tradition of awards to those simulation pioneers**





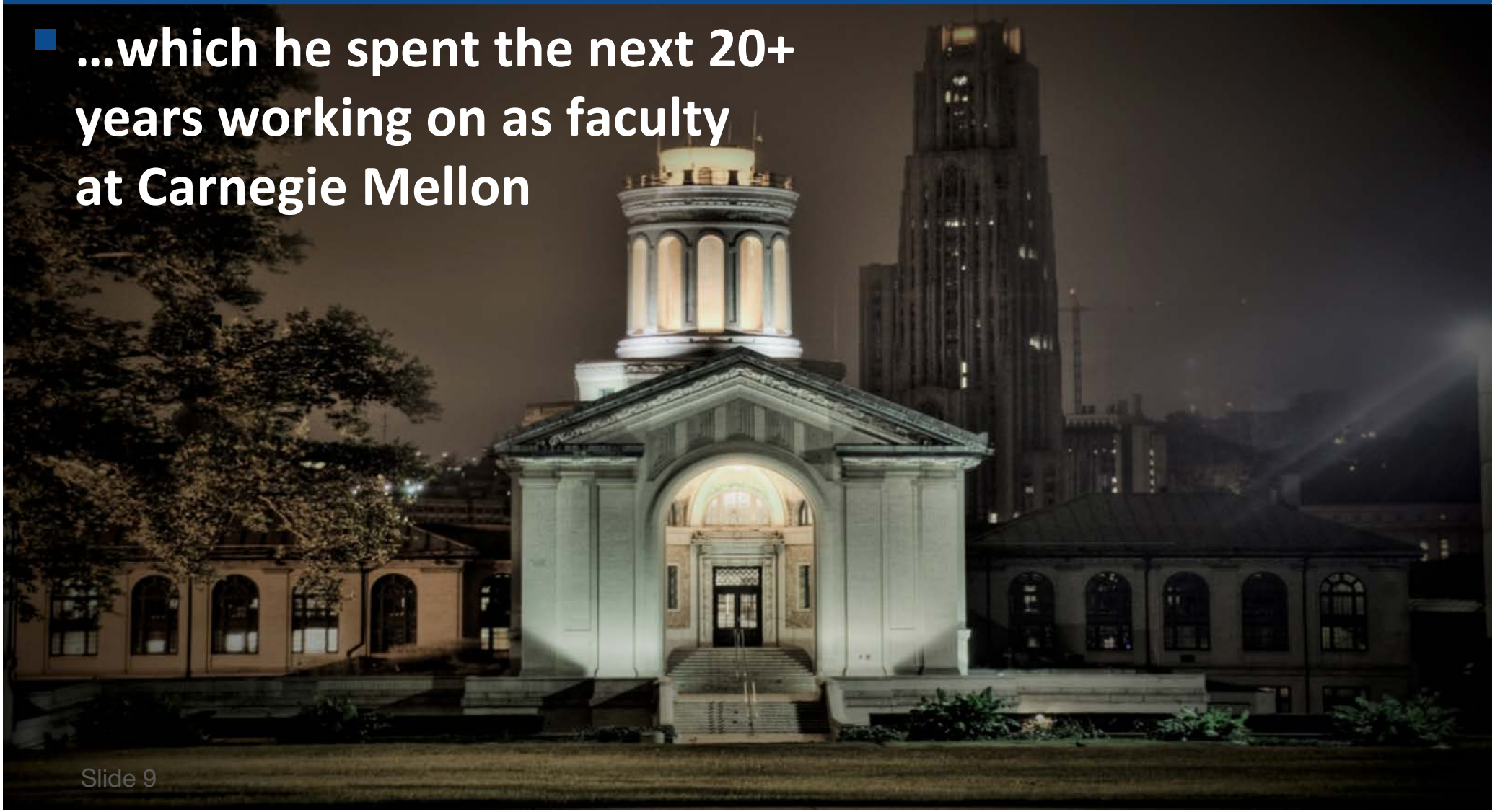






But Rob Saw a Large Opportunity

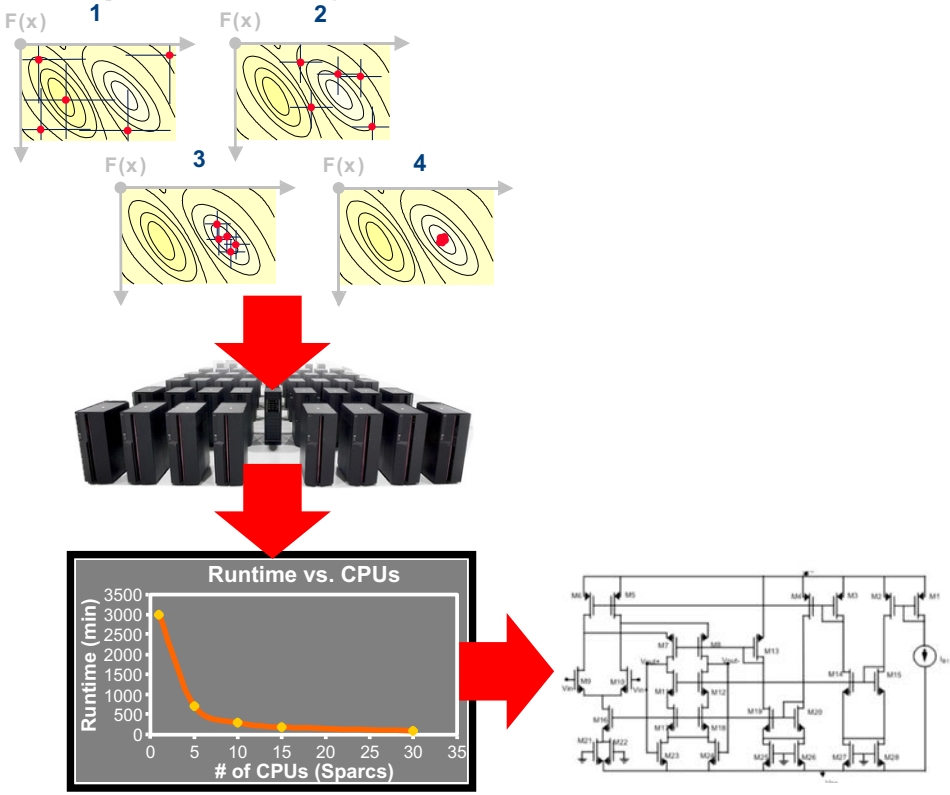
- **…which he spent the next 20+ years working on as faculty at Carnegie Mellon**



Rob's Big Idea

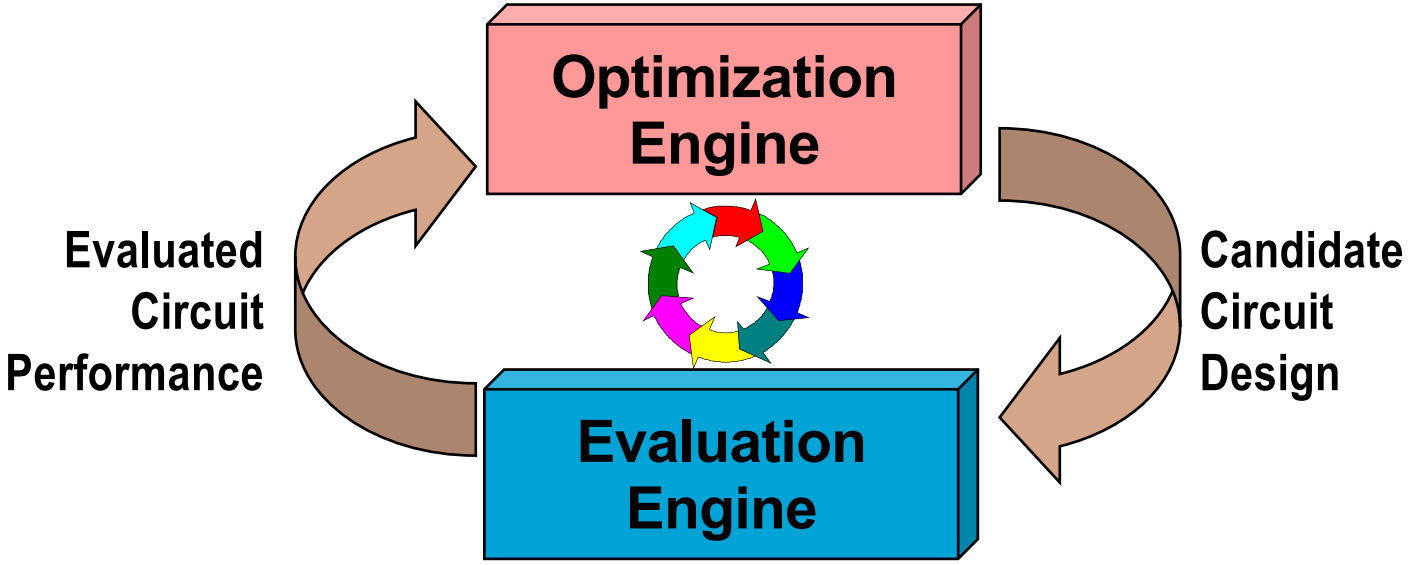
- **Analog – it's *art*, it's *deep*, *mysterious*, *painful*, *sublime*…**

- **NO – it's *optimization*. Big hard optimization.**

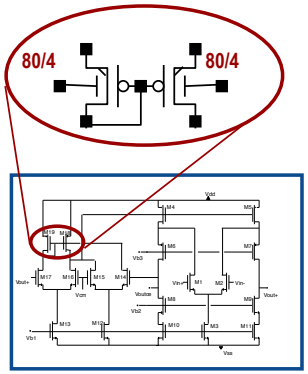


Rob's Big Idea, Revisited

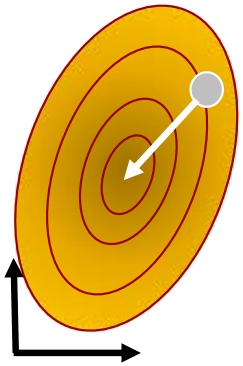
- **Clever models & engines can support *principled search* for best analog design to *meet designer constraints***



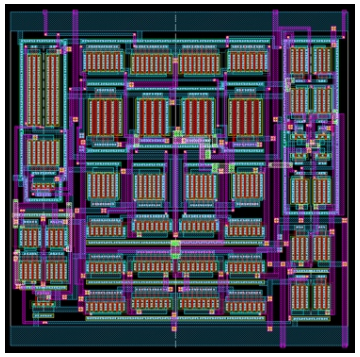
Pursued Across Breadth of Analog



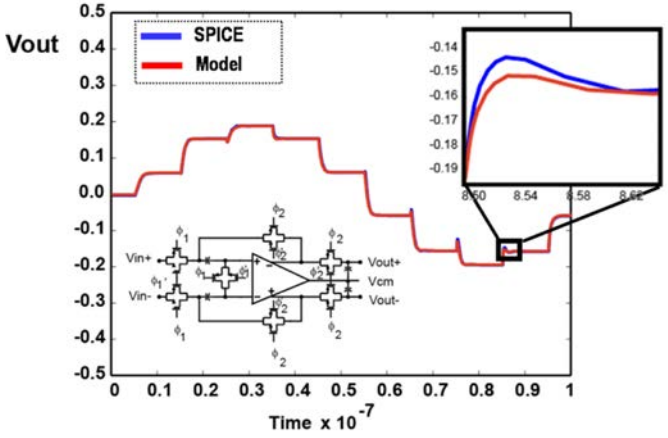
SIZING



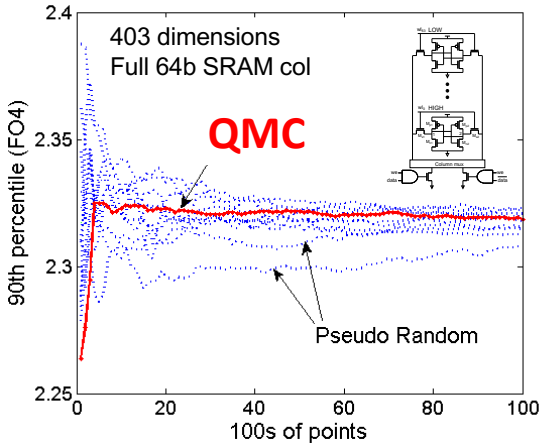
OPTIMIZATION



LAYOUT



MACROMODELING

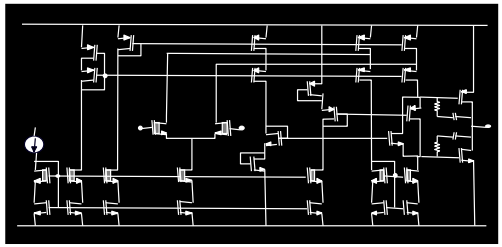


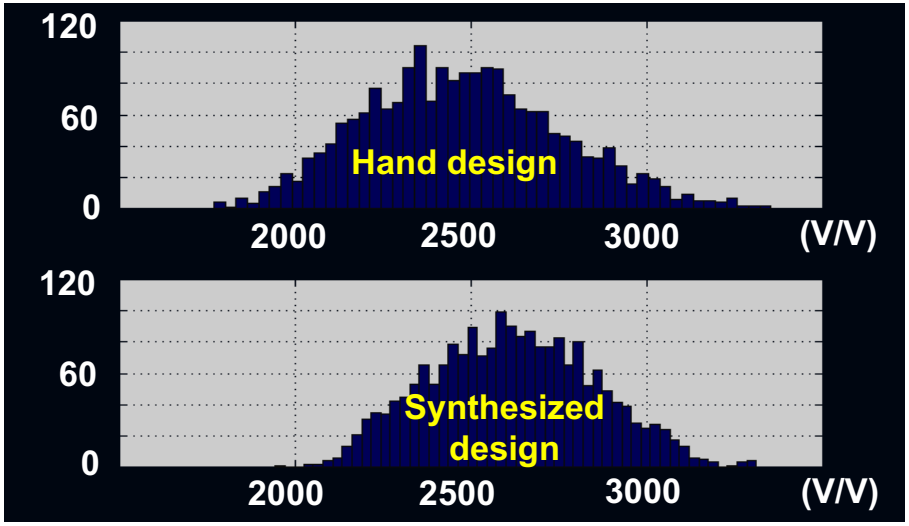
STATISTICS

●●●

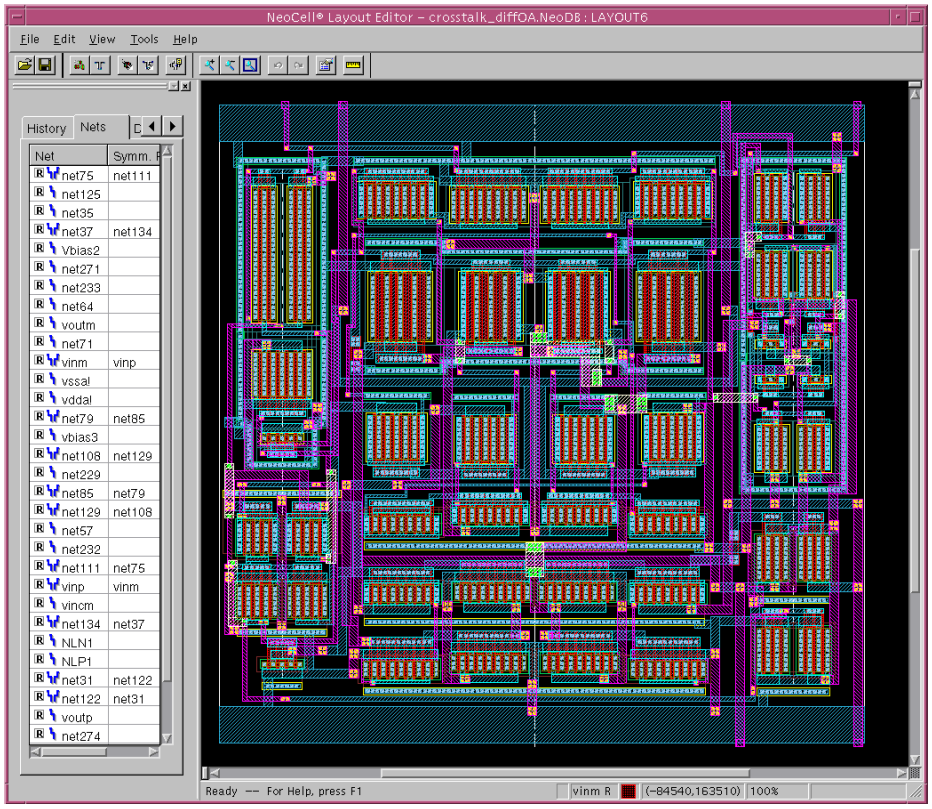
Two Analog Examples

- **Practical Spice-in-the-Loop optimizers that "just work"**



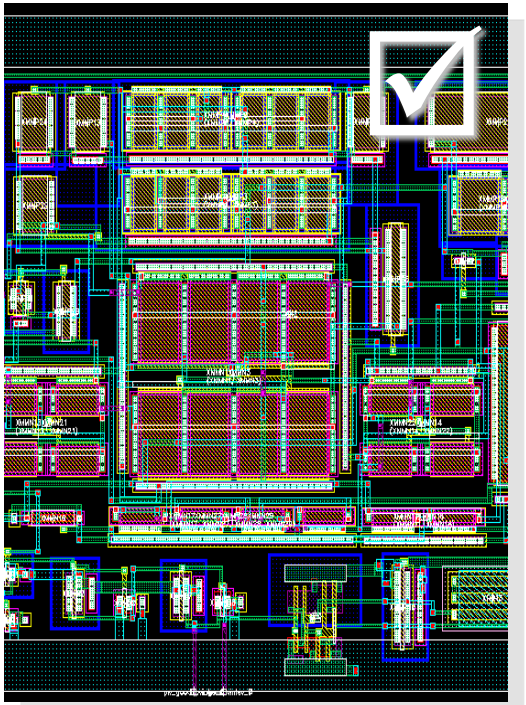


- **Automatic layouts with manual aesthetics & performance**

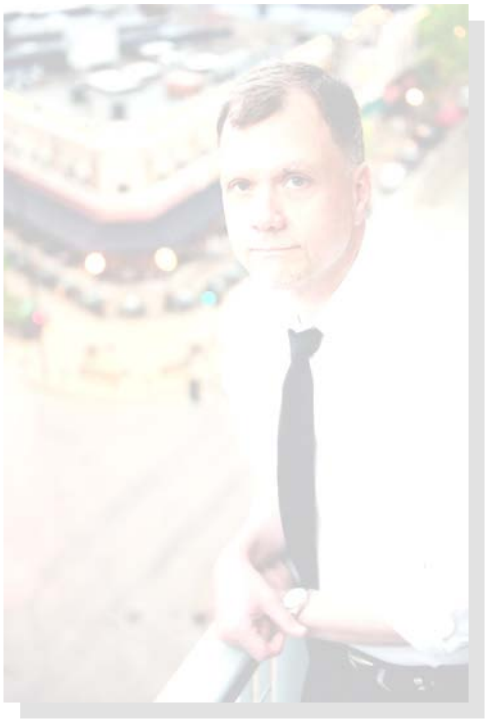


An Appreciation, in Three Acts …

The ideas

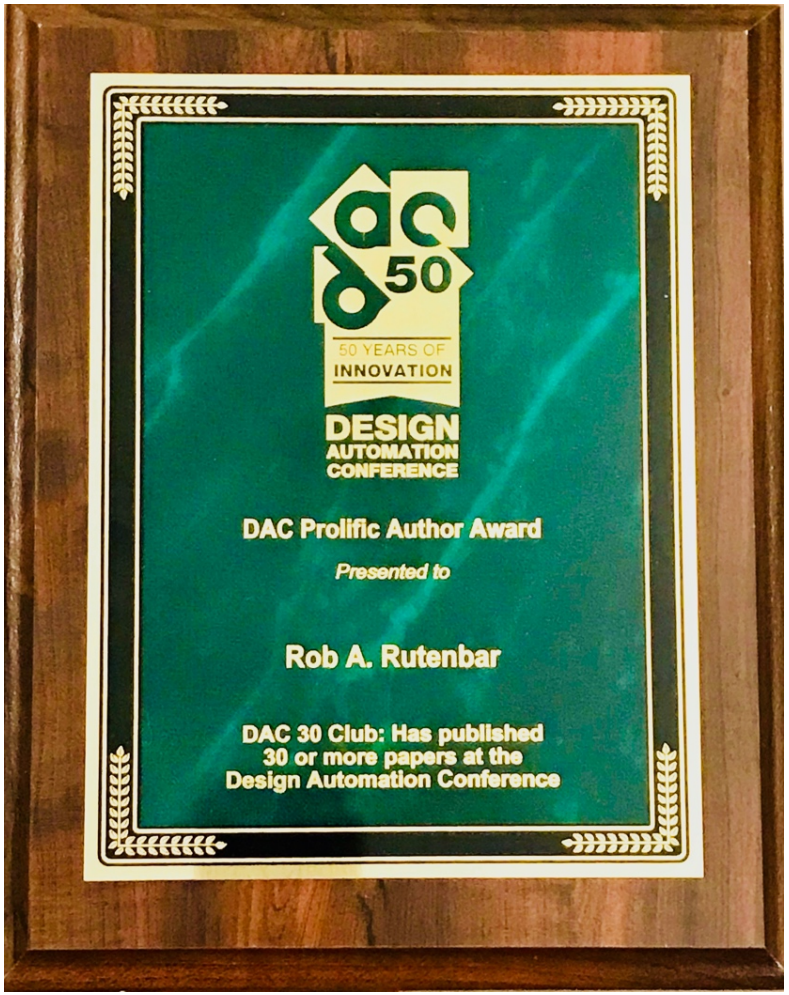


The impact



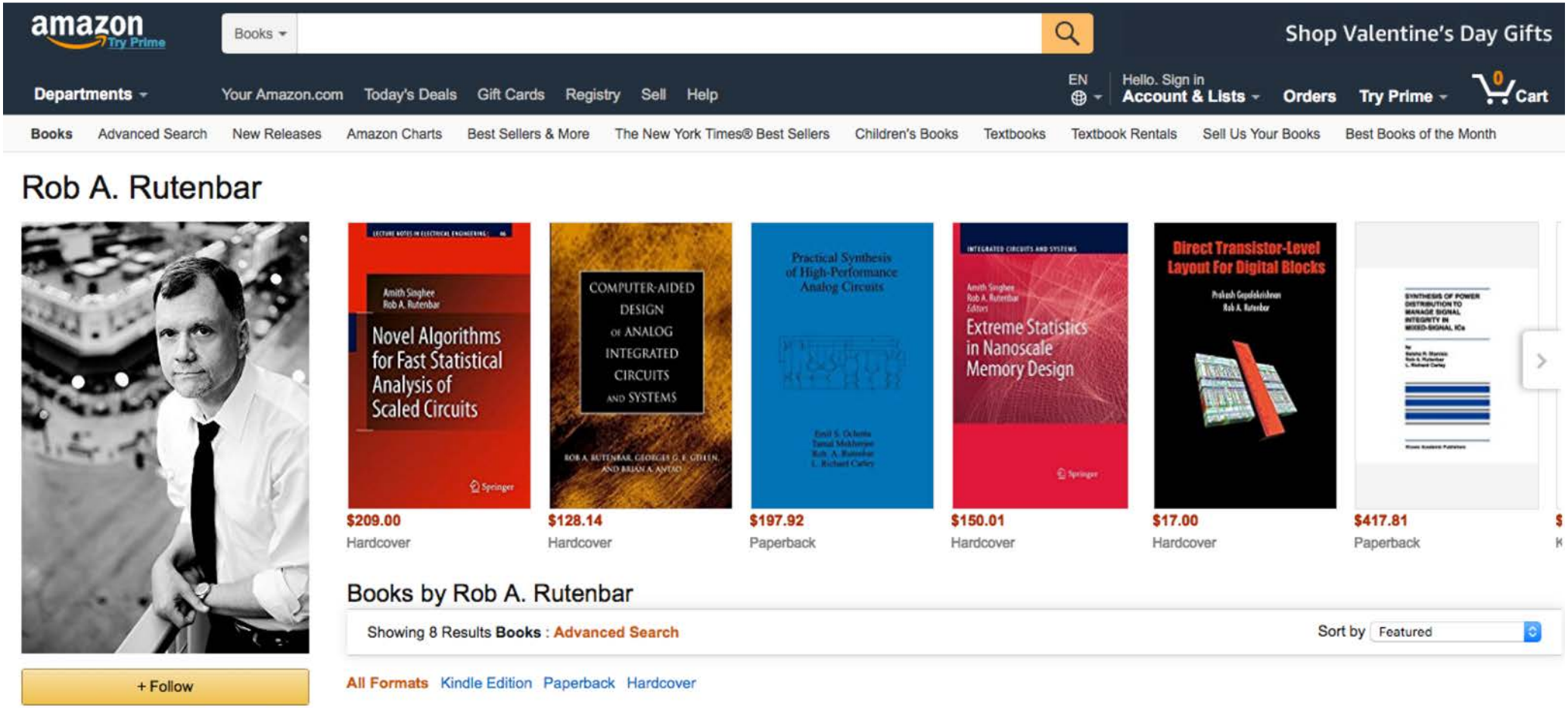
The individual

Academic Impact (Of Course)



- **200+** papers, books etc
- **~10,000** citations
- Many, many awards
  - **3** DAC Best Papers
  - **2** IEEE TCAD Pedersen Awards
  - **1** DATE Best Paper
  - **1** ICVLSI Best Paper

Rob Really “Wrote the Books” Here

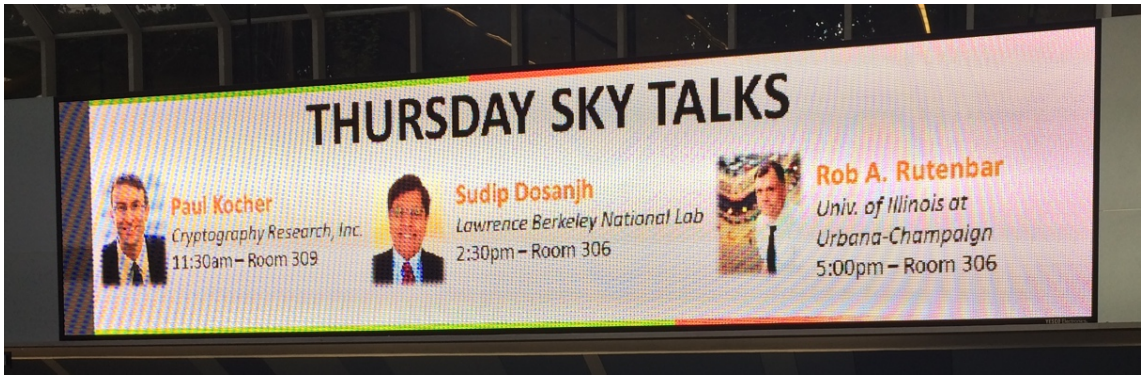


Contributed to EDA & Tech Community

EE Times Connecting the Global Electronics Community

SIGNALS

Synthesis proves to be Holy Grail for analog EDA



51 DESIGN AUTOMATION CONFERENCE

More Critically – Deep Industry Impact

neolinear

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Chief Technologist

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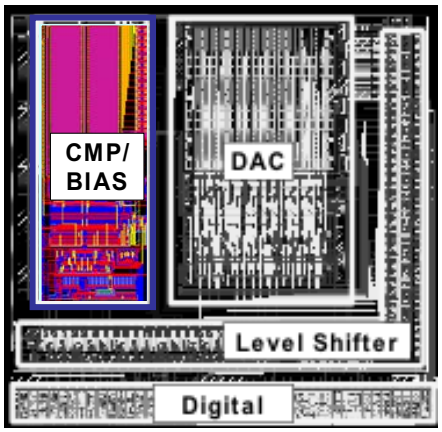
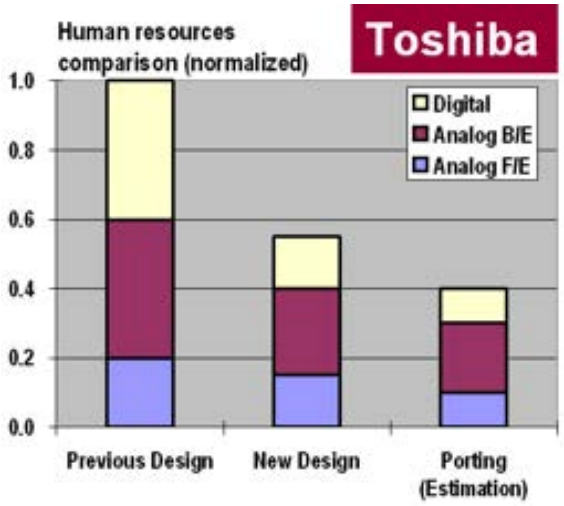
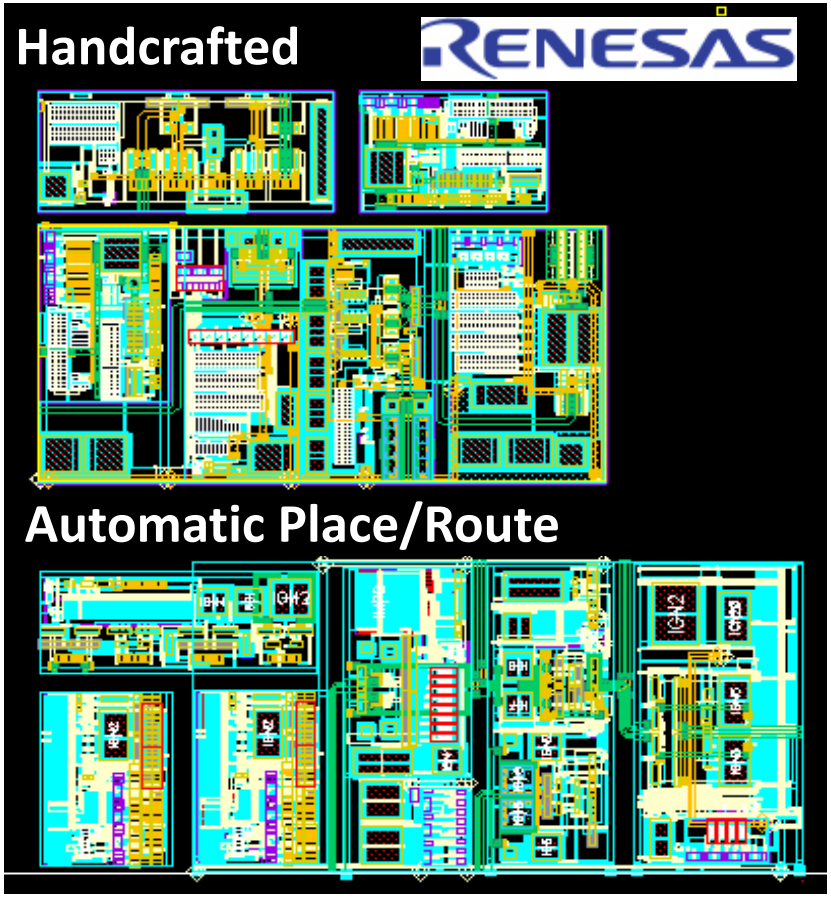
311 South Craig Street
Suite 102
Pittsburgh, PA 15213
Tel 412.681.1080
FAX 412.681.0802

rutenbar@neolinear.com

Neolinear: Front-to-Back Analog Tools







Neolinear: Customers

NeoCircuit & NeoCircuit-RF

NeoCell

2004: Neolinear → Cadence

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Financial News

Enter symbol(s) Basic Get

Press Release Source: Cadence Design Systems, Inc.

Cadence to Acquire Neolinear

Tuesday April 6, 8:30 am ET

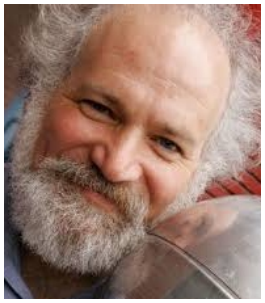
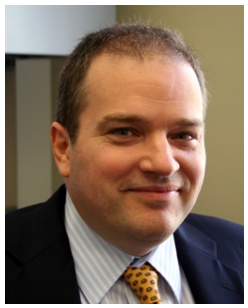
Neolinear Technology to Accelerate Design Cycle and Enhance Silicon Yield

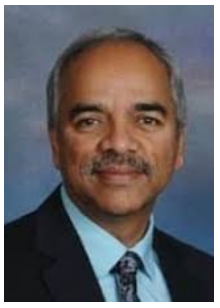
SAN JOSE, Calif.--(BUSINESS WIRE)--April 6, 2004--Cadence Design Systems, Inc. (NYSE:CDN - News) today announced it plans to acquire Neolinear, Inc., a privately held company. Neolinear's rapid analog design technology is critical for the consumer and communications markets where semiconductors are increasingly differentiated by their analog content. The Neolinear team will bring additional strong A/MS and RF expertise into Cadence and play a key role in driving ongoing innovations for improving yield and speeding IP reuse in the Cadence® Virtuoso® custom design platform. Neolinear's NeoCircuit and NeoCell are already an extended part of the industry-leading Virtuoso platform through an OEM agreement between the two companies.

Now: Cadence Pittsburgh

But Also Another Impact: Teaching

- **Rob is an extraordinary, dedicated teacher**
- **His CMU class alums are a Who's-Who of EDA leaders**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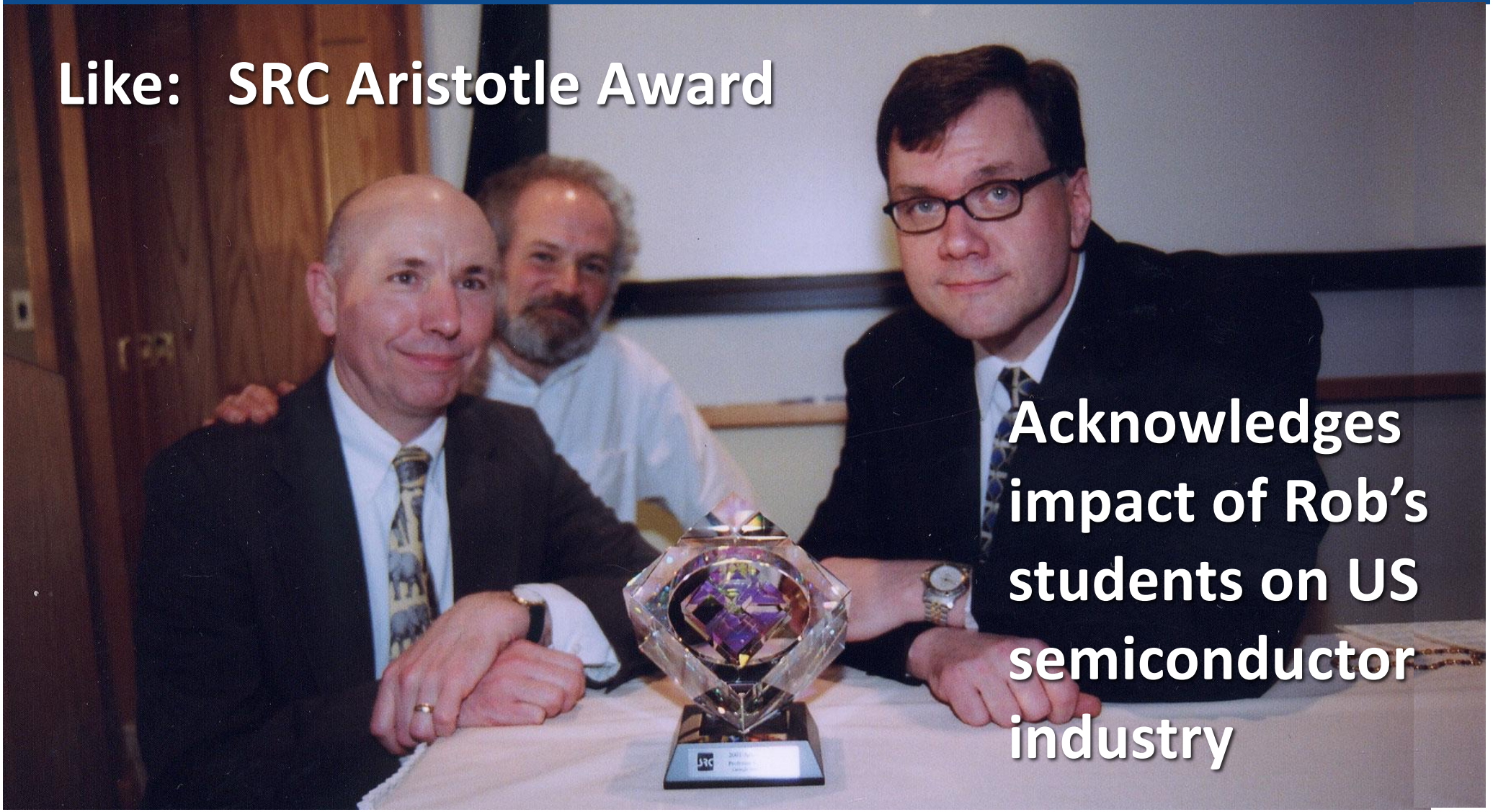
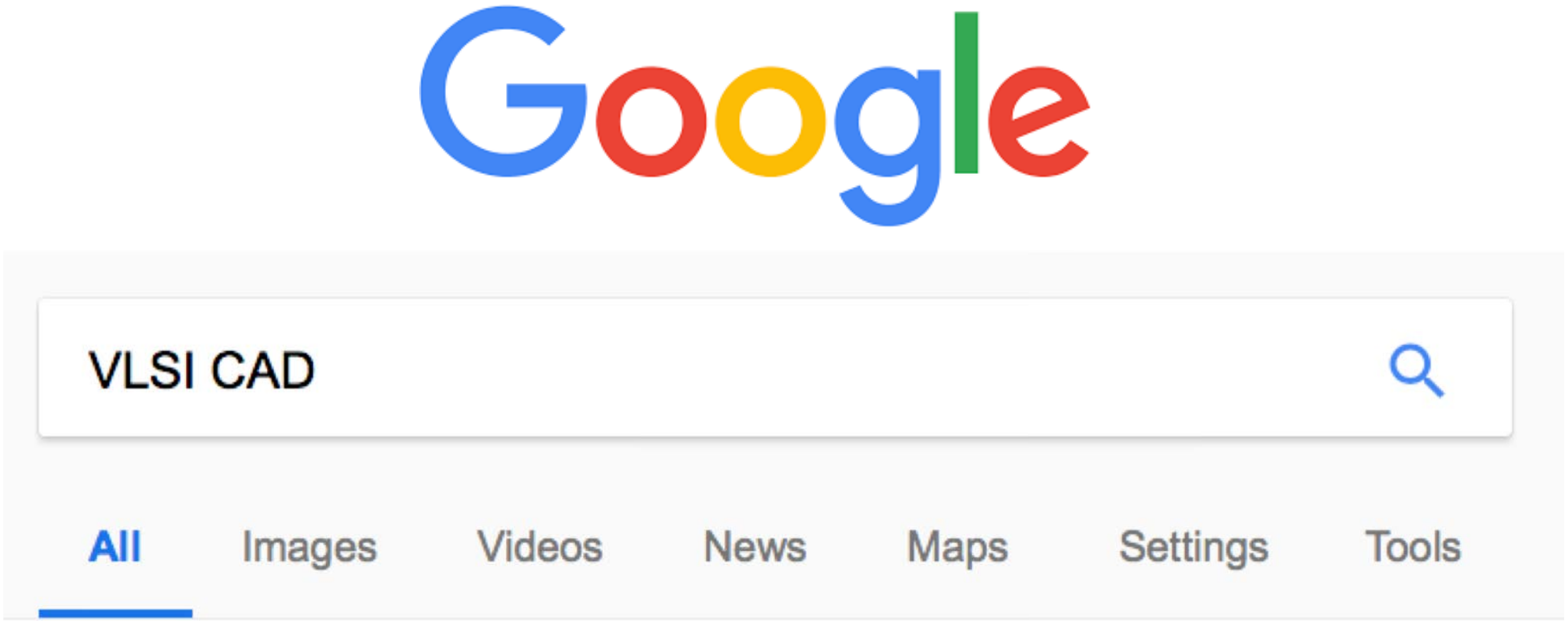
Won Major Teaching Awards



Another Measure of Impact

- **What happens when you type this…?**



Answer: You Get **Rob** (8 of Top 10!)

About 341,000 results (0.39 seconds)

#1 Rob's MOOC

VLSI CAD Part I: Logic | Coursera
https://www.coursera.org/learn/vlsi-cad-logic
About this course: A modern **VLSI** chip has a zillion parts -- logic, control, memory , interconnect, etc. How do we design these complex chips? Answer: **CAD** software tools. Learn how to build thesA modern **VLSI** chip is a remarkably complex beast: billions of transistors, millions of logic gates deployed for computation and ...

#2 Rob's MOOC

VLSI CAD Part II: Layout | Coursera
https://www.coursera.org/learn/vlsi-cad-layout
About this course: You should complete the **VLSI CAD** Part I: Logic course before beginning this course. A modern VLSI chip is a remarkably complex beast: billions of transistors, millions of logic gates deployed for computation and control , big blocks of memory, embedded blocks of pre-designed functions designed by third ...

#3 *Bootleg* of Rob's MOOC

VLSI CAD: Logic to Layout Lecture 001 Welcome and Introduction ...


https://www.youtube.com/watch?v=WLdbujc-aH4
Mar 11, 2013 - Uploaded by Alireza Saberi
Alireza Saberi. ... Course is presented by professor Rob A. Rutenbar is the Abel Bliss Professor and ...

#4 *Review* of Rob's MOOC

Reviews for VLSI CAD Part I: Logic from Coursera | Class Central
https://www.class-central.com › Coursera
★★★★★ Rating: 5 - 3 reviews
A modern **VLSI** chip has a zillion parts -- logic, control, memory, interconnect, etc. How do we design these complex chips? Answer: **CAD** software tools. Learn how to build thesA modern **VLSI** chip is a remarkably complex beast: billions of transistors, millions of logic gates deployed for computation and control, big blocks of ...

Reminder: **M**assive **O**pen **O**nline **C**ourses

Internet-scale video
(for instruction)

+

Cloud-based assignments
(for eval & grading)

+ Super Cheap = **MOOCs**

In 2013, Rob Launched First EDA MOOC

- **And, its been running ever since, including right now…**

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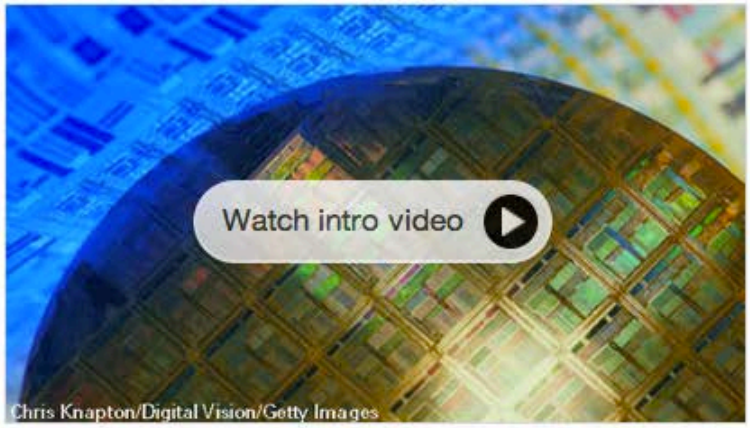
ILLINOIS

VLSI CAD: Logic to Layout

Rob A. Rutenbar

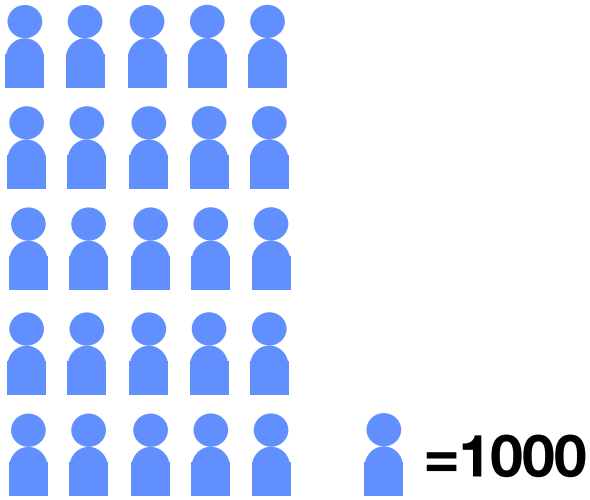
A modern VLSI chip has a zillion parts -- logic, control, memory, interconnect, etc. How do we design these complex chips? Answer: CAD software tools. Learn how to build these tools in this class.

Workload: 10-12 hours/week

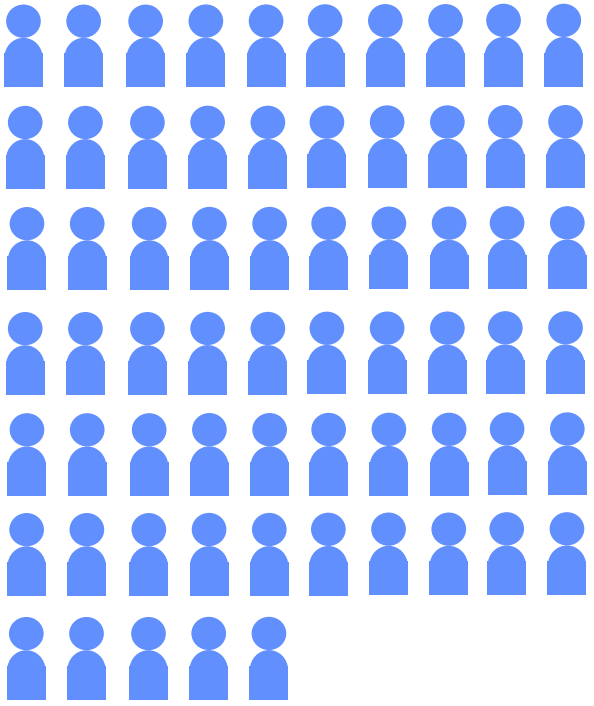


EDA MOOC Impact

- **It is estimated there are roughly 25,000 EDA professionals on the planet**

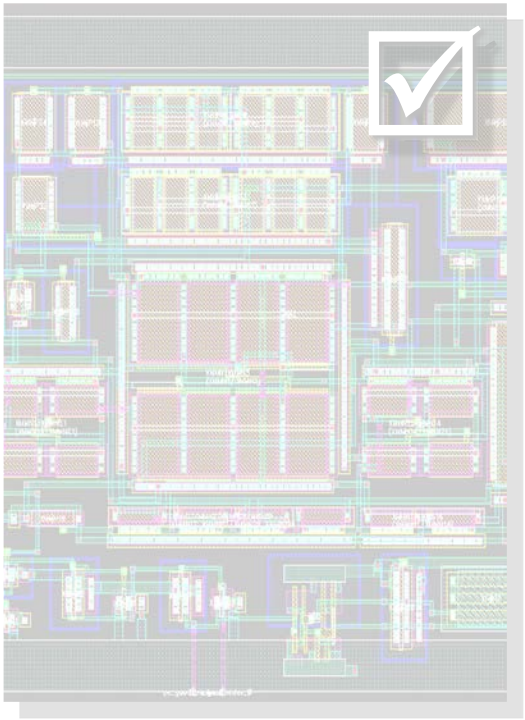


- **Rob's MOOCs, since 2013, have enrolled 64,310 of them (~100 more every week)**



An Appreciation, in Three Acts …

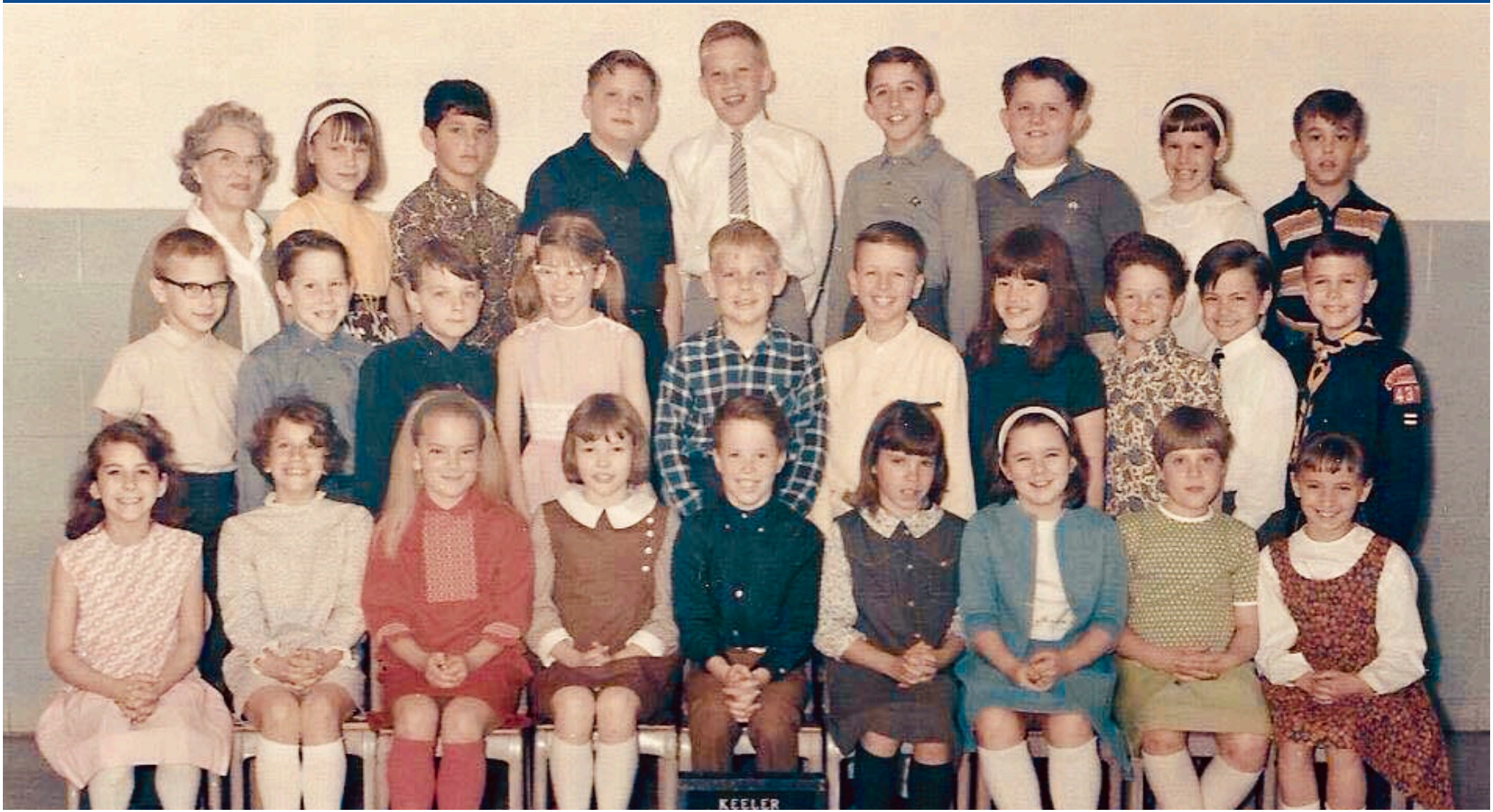
The ideas



The impact

The individual

Just Another Kid from Detroit…



Rob: Five Schools, Forty Years

‘75-’78 Wayne (BS)

Wayne State University

‘78-’84 Michigan (MS, PhD)

University of Michigan

‘84-’09 CMU (Faculty)

Carnegie Mellon University

‘10-’17 UIUC (Head)

ILLINOIS

’17-now Pitt (VC Research)

University of Pittsburgh

Prof. Rutenbar → Manager/Boss

- **Head of CS** at University of Illinois at Urbana-Champaign

- **Vice Chancellor for Research** at University of Pittsburgh

New Friends, New Challenges

Rob's Key **Nontechnical** Achievements

Rob Rutenbar: 2017 Kaufman Award