DAC at 50: The Second 25 Years

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How does one survey a quarter century of technical contributions at a world-class venue like the Design Automation Conference? This was the daunting challenge I faced when asked to survey the second 25 years of DAC’s history at the 50th anniversary conference event in 2013.

One can imagine several strategies, for example:

- Identify a set of “greatest hits” technologies and methods. There were assuredly many such breakthroughs across these years. But how to winnow the list to something of manageable length, without slighting an important idea or innovation?
- Identify a set of “most important EDA tools” from these years. The way we make impact is to deliver working software and flows to our friends in the design community. But this underweights the long and winding path through ideas and experiments published at DAC, whose exploration necessarily precedes each delivered tool.
- Identify a set of the “most important EDA startups” from these years. Our industry has been a vital one because of its active entrepreneurial ecosystem, engaged broadly across academia, startups, and larger established EDA companies. But again – who makes the list, and who does not?

Attempts to enumerate “Best Of...” lists seem destined to miss something vital. I decided this survey needed a better idea.


Today, everyone working in information-related fields is part of the “Big Data” revolution. Data as these new scales dramatically changes the ways we interact with technology, among other things. A central tenet of the data revolution is the idea of letting the data speak for itself – that is, diving deeply into these raw information streams and pulling out the patterns we find there.

This suggests an approach for our survey task. Let’s consider the “source data” as the set of all papers published at DAC over these second 25 years. This is DAC 1989 to DAC 2013 (though, for expedience, I only surveyed up to 2012). Figure 1 shows the raw paper counts across these years. I do not count the myriad special sessions at DAC, since these are difficult to label in terms of their technical focus. (For example, panel sessions often comprise a range of conflicting views on technical
matters.) I looked at the papers in each session, and then categorized the entire session itself as being part of one specific technical area, e.g., synthesis, layout, power, codesign, nanometer effects, etc. I tracked paper counts across each technical category, across all years. In this way, I categorized every paper – almost 3900 such papers – across all these years, by their technical focus.

These categories are, of necessity, the author’s choice, and so may exhibit some unintentional biases. I tried very diligently to maintain a broad and balanced outlook across these papers, and to use category labels that were widely understood by the general DAC audience and EDA community. And, of course, any errors of counting are my responsibility.

I believe the final results are extremely illuminating. My starting hypothesis was that the broad technical areas of EDA – as measured by paper counts – would tell the overall narrative of what each year was like in our community. Some years were calm, some were hectic – even panicked. Problems broke into the consciousness of the DAC community, and solutions arose to combat them. Technical areas were born and grew, and dominated the scene for some number of years. But then just as naturally, they ebbed, as the core problem they addressed was solved. Some areas effectively disappeared, but just as often, groups of related sub-areas merged into a new area with a different, refreshed focus.

I believe the paper count data does a lovely job of telling the story of the second 25 years of DAC. To narrate this story in a clear way, I have broken the data into a set of five half-decade “acts” (with due apologies to Shakespeare), and show the category/count data by technical area for each of these 5-year epochs.

ACT I, DAC 1989-1993: Age of the Core Flow

Figure 2 shows a first attempt to count and categorize our first 5 year epoch. The technical areas are, I think, well understood: Design environments, RTL & languages, High-level synthesis, Logic synthesis & mapping, layout, etc. But while the data might naturally fall into 15-20 finely partitioned categories (there are 14 such categories in this Act), I quickly discovered this was too much detail from which to pull out key trends driving the industry and community.

Figure 3 shows my proposed solution: another round of categorizing, clustering, and counting, to reduce this fine-grain data to a handful of macro trends. At this level of detail, the big trends are clear and crisp. This is the age of the “Core Flow,” where the DAC community built the foundational synthesis and verification techniques that allow us today to push a button, and turn 50,000 lines of Verilog into 1M gates of working, reliable logic. There are four big areas in this act:

- **Core Synthesis:** work focused on databases and design environments, on RTL language issues, behavioral synthesis, logic synthesis and tech mapping.
• **Core Verification**: work focused on both logical and electrical (circuit) simulation, on test, and on the real beginnings of formal methods.

• **Trending Timing & Interconnect**: we see clearly the beginnings of growth in this as an area of concern, as designs became larger, ran faster, and began to be realized in less friendly scaled technologies.

• **Emerging FPGA & Analog**: we also see clearly the emergence of new non-ASIC areas of focus. This act is the real start of both FPGAs and analog and mixed-signal EDA tools as serious areas of inquiry for the community.

There were numerous important “firsts” in this epoch. Many new data structures and algorithms. Work across all levels of the design hierarchy: gates, transistors, shapes. Breakthroughs in formal methods involving Binary Decision Diagrams and model checking. The first moment methods to analyze the electrical delay of wires. The first accurate probabilistic models of switching for power estimation of logic. The first descriptions of scripting-based languages designed to create complex design flows. From our vantage point twenty years later, it is quite satisfying to see how many of these early ideas actually “got real” in today’s tools and flows.


Figure 4 shows paper counts and categories for this next act. To focus on the critical emerging trends, I cluster some separate areas from the previous epoch in this new chart. So, synthesis and layout are now clustered as one very important area – indeed, the largest single area. But this is also clearly an area that was gradually shrinking in these years, a victim of its own stunning successes.

Verification and test remain important, though we note the rise of the term “functional verification” in this era, emphasizing that the end goal is to make our systems *function*, and not just watch waveforms on transistors and gates. We also cannot ignore the emergence of formal verification as an area of sufficient substance to make it into our category list. FPGAs and analog continue to be areas of interest, but they have not yet “broken out” as bigger focus topics for DAC in these years. The new emergent area is embedded systems. We see in these years the rise of embedded computing as a separate area, with a range of modeling, optimization, estimation, and codesign problems that merit its own category in our count.

But the real story here is the focus on timing, interconnect, and power. Figure 5 tries to highlight these key trends by focusing on just these categories, and the related area of design case studies, labeling the paper counts by the targets of optimization: *MHz, Watts, cost, complexity*. This is the age of “Deep Submicron” (DSM), the era when the core flow of the previous era stopped working. These were scary years for our readers who did not live through them. Starting at around the 130nm or 90nm CMOS nodes, our cherished synthesis, layout, and timing/power closure solution began to fail. Previously, we could synthesize logic,
ignoring the subsequent physical layout, and the fact that wires themselves had complex shapes, and real delay. Simple expedients like overdesign, timing margins, a few “extra buffers” to fix recalcitrant critical paths, failed in the face of designs with many more gates, on much larger die, operating at much greater clock speeds. Many ASICs could not be “closed,” that is, that could not be tweaked to meet timing. Worse, when tweaked, the resulting power was unsupportable. Many chips died an ignoble death, moving through respin after respin, chasing a timing/power target that was never to be. Many such design teams simply ran out of funding before the chip ever reached the market.

Figure 5 shows clearly the emergence of the DSM closure crisis; by 1998, fully a third of the entire DAC conference was focused on these topics. Case study sessions alone were hugely popular, as grizzled veterans of the DSM wars shared horror stories, news of hard-fought battles, and tactical techniques to avoid getting killed oneself. The good news from this rather dire narrative is, of course, that we fought the battle, and we won. The DAC community marshaled its efforts, focused its immense talents on the problem, and progress was made. To cite just one example: we now understand what a term like “physical synthesis” means. That logic synthesis must take basic account of layout geometry, of likely wiring problems, and the overall physical design. And layout design must be able to re-synthesize and retime problematic blocks to meet difficult specification. And that timing and especially power are metrics that must be integrated into every step of the core flow.


Figure 6 shows paper counts and categories for this next act. As before, to focus on the key trends, I cluster areas from the previous epoch in this new chart. Thus, synthesis, layout, verification and test are now clustered as one “super area,” accounting for fully a third of the total DAC paper count. This is our new “core flow” for the new century, responsible for continued focus on the basic foundation of techniques to build and validate the increasing complex designs of the era.

Likewise, timing and interconnect have been merged into a super-area called “closure,” to recognize the impact of the DSM crisis on the entire EDA community. The story behind the power area in Figure 6 is a bit nuanced. The trend line suggests a diminution of interest; this is emphatically false. What actually happens here is that fewer DAC sessions are uniquely about power, while more DAC papers simply embrace power as an essential topic that must be included. Said differently: almost all the papers start touching on power issues, in some way.

The clear emerging area is around nanometer effects, which appear in this epoch for the first time, in a big way. In these years, we stop saying “deep submicron,” and we start saying “nanometers”. Lithography papers appear. Models of the statistical
problems with variable process parameters, especially threshold voltage, appear. There is the first tentative discussion of an “end of roadmap” scenario for CMOS and Moore’s Law.

The clear breakout trend, however, is the rise of system design concerns, across a great range of heterogeneous platforms. Figure 7 highlights these areas, again labeling the trend counts with the targets of these many papers. We see in these years a great blossoming of EDA for a new range of targets: not just ASICs but also ASIPs; not just digital but also analog and mixed-signal and RF; not just FPGAs but also a broader range of reconfigurable platform designs; and a broad and mature view of hardware versus software issues across all of these platforms. To cite just one celebrated example, the very first work on Network-on-Chip architecture appeared at DAC in 2002, in the middle of this explosion of heterogeneity.

ACT IV, DAC 2004-2008: Age of Uncertainty

Figure 8 shows paper counts and categories for this next act. As before, some super-areas appear as clusters of separate topics in the prior era. The core flow super-area dominates roughly 40% of the conference, and now also includes topics in power and thermal management, which are spread widely among synthesis, layout, and verification topics. The systems area is also substantial, and includes a broad array of work on embedded, SOC, multicore, reconfigurable and analog platforms.

An interesting new area arises: Communication. For the first time, there are entire sessions about SOC-scale communications architectures, focusing on networking, busses, communication protocols, IP and the like, for how to get information from one end of a huge chip to the other.

Nanometer effects also occupy a notable fraction of the conference, with the addition of new focus on reliability and post-silicon debug as novel topics. We see the first papers on EDA issues working to ensure that, after manufacturing test, designs do what we expect them to over their lifetime. Likewise, we see the first EDA tools to address issues in post-silicon debug and tuning, as chips increasingly require “tweaks” post-fab. Emerging technologies – either non-silicon or post-silicon – also become more prominent as topics of real EDA concern in this epoch. This is the era in which the reality of an end to Moore’s Law scaling was finally accepted as a fact of life.

Figure 9 shows an attempt to capture the macro trends in this area. When one looks carefully at the full range of publications, the one striking pattern is the rise of probability and statistics as the foundational mode of thinking about most EDA problems. Thus, I am tagging this as the “age of uncertainty”. Foundry fabrication parameters are statistical and uncertain. Yield, timing and power are uncertain.
Communications are uncertain. Chip reliability and post-debug performance is uncertain. This is the era of the demise of determinism, the era when everything interesting is a random variable, or a correlated smear of probability. Yet, even in this new and challenging milieu, the EDA community made substantial progress. Design became uncertain, but we became proficient in building statistical models that let us cope. Finally, one other related “uncertainty” area rose to prominence in this era: security. We saw the first papers on security issues as being topics of fundamental interest to EDA tools and platforms. And we saw the first steps toward addressing trust issues in semiconductor supply chains: if my chip is designed here, and fabricated there, and used yet elsewhere, how do I trust that it was not tampered with?

**ACT V, DAC 2009-2012: Age of Applications & Adjacencies**

Figure 10 shows paper counts and categories for this final act. (I note for completeness that our final epoch leaves us one year shy of the full 25 years promised, based on the timing required for the preparation and delivery of this analysis at DAC50 in 2013.) Two super-areas comprise roughly half of the whole DAC universe: the core flow (synthesis, layout, verification, test), and the broad nanometer variability area (including reliability and debug). This comes as no surprise: the core flow is always the target for some form of improvement, and in today’s designs, it is the nanometer effects that dominate. Trust and security, and 3D packaging also appear as an area of note.

But the breakout areas in this final act focus on applications, as shown in Figure 11. This is the age of “applications and adjacencies”. Applications have always driven the design community, and as a consequence the EDA community. We focus on embedded power, for example, because of the explosion of mobile appliances. But looking in detail at the DAC papers from this era, one sees a dizzying array of diverse new applications: mobility, computing, communications, security, energy, cloud, health, medicine, etc. And one sees attempts to wrestle with the landscape of emerging technologies in both the post-silicon and non-silicon worlds. We have always focused our efforts on systems, but in this area, it is largely the applications that drive the system architectures, which then drive the EDA focus.

This is also the age of “adjacencies,” by which I meet the business opportunity of adjacent markets. Are there design problems with a similar level of complexity, chain of abstractions, interplay of hardware and software, requirements for fresh design and desire for IP reuse? Might we take what we know of semiconductor oriented EDA and direct it toward these adjacent opportunities? The automotive industry is one key adjacency opportunity that appears frequently in these years. Medical appliances is another.
The striking takeaway from looking at DAC in this most recent epoch is the combination of a mature technology base – the flagship core flows we have created, our growing mastery of nanometer “unpleasantness” at the end of Moore’s Law – and the exciting, broad exploration of new domains and new industries where we might be able to apply not just our tools, but our overall worldview for solving huge and difficult problems.

Conclusions

I must admit that, when I accepted the invitation to undertake this survey, I did not plan on individually perusing approximately 4000 separate DAC papers and related panels and special sessions. Nevertheless, I am happy with the results of this experiment. The trend charts shown in Figures 2 through 11 show a vibrant community growing and adapting, wrestling with huge challenges, and surmounting them. I am quite optimistic about the future of the next 50 (and more) years of the EDA discipline.
Rob A. Rutenbar received the PhD degree in 1984 from the University of Michigan, and spent the next 25 years on the faculty at Carnegie Mellon. At CMU, his group pioneered tools for custom analog circuits. In 1998 he cofounded Neolinear. Inc., to commercialize this work, and served as Chief Scientist until its acquisition by Cadence in 2004. He has also worked extensively on nanoscale silicon statistics. In 2010 he moved to the University of Illinois at Urbana-Champaign, where he is Bliss Professor and Head of Computer Science. He has won numerous awards in his career, including three DAC Best Papers. He won the 2001 SRC Aristotle Award, acknowledging the impact of his students on the US Semiconductor industry. Most recently, he shared the 2013 Donald O. Pederson Best Paper Award for IEEE Transactions on CAD. He is a Fellow of the IEEE and the ACM.
FIGURE 1

Count of technical papers published at DAC from 1989 to 2012.
Figure 2

ACT I, DAC 1989-1993. Paper counts and categories. (This and subsequent figures for each “Act” omit detailed paper counts to emphasize that the focus is on temporal trends (rises and falls) and relative trends (one area’s size versus another’s.)
Figure 3

ACT I, DAC 1989-1993 Revisited: Age of the Core Flow
Figure 4


DAC Paper Count

- FPGA & ANALOG & OTHER
- TRENDING: Embedded
- DESIGN CASE STUDIES
- POWER
- TIMING & INTERCONNECT
- FORMAL VERIFICATION
- FUNCTIONAL VERIFICATION & TEST
- CORE SYNTHESIS & LAYOUT

Figure 5


DAC Paper Count


DM $\\$ Complexity Watts MHz Nanoseconds

DSM CLOSURE CRISIS
**Figure 6**


![DAC Paper Count](image)

- **EMERGING:**
  - nm effects, litho, leakage, variability
  - End of CMOS

- **RECONFIG & ANALOG**

- **SYSTEMS:**
  - Embedded, Hw/Sw, SOC, IP, Reuse

- **POWER**

- **CLOSURE: TIMING & INTERCONNECT**

- **SYNTHESIS & LAYOUT**

VERIFICATION & TEST

1999 2000 2001 2002 2003
Figure 7


DAC Paper Count

ASIC & ASIP
Hardware & Software
Digital & Analog
Fixed, Programmable, Reconfig
Figure 8

Figure 9

ACT IV, DAC 2004-2008: Age of Uncertainty

What’s my $V_T$? Timing? Yield?
What’s at end of CMOS? After?
How many mW for my code?
Can I trust your fab, your chip?
Figure 10

ACT V, DAC 2008-2012: Paper counts and categories

- EMERGING TECH & APPS
- SYSTEMS
- 3D / TRUST+SECURITY
- NM: VARIABILITY
  NEW: RELIABILITY / DEBUG
- SYNTHESIS & LAYOUT
  VERIFICATION & TEST
  THERMAL & POWER

[Graph showing paper counts and categories from 2009 to 2012]
Figure 11

ACT V, DAC 2008-2012: Age of Applications & Adjacencies

What device technology?
What implementation fabric?
What end-user domain?
Programmed? reconfigured?
What EDA will this need?