What’s Up With Analog (CAD)…?
A Talk in 3 Parts

- Looking back: Analog CAD history in review
- Reflection: What we got right (& not...)
- Looking forward: New opportunities
A Little Analog History...

- In first decade (more or less) of 21st century, lots of startups doing first ‘real’ products, based on previous decade of R&D
A Little History...

- Most of them died; a few got bought by big EDA players; technologies added to big, flagship analog/mixsig platforms
We Made Some Real Progress

Digital Methodology
- Synthesis
- Optimization
- Verification
- Reuse & IP

Analog Methodology
- Toward Synthesis
- Toward Layout
- Toward Stats Optimize
- Toward Reuse & IP
Core Strategy: Optimization-Based Design

- All successful approaches have this overall structure

- Use some clever form of heuristic or numerical search
  - **Optimization engine:** proposes candidate circuit solutions
  - **Evaluation engine:** evaluates quality of each candidate
  - **Cost-based search:** cost metric represents “goodness” of design
Key Example: Sizing/Centering Tools

- For device-level ckt design, you have to do these tasks

Generate proper specs

Design proper circuit topology

Design proper device sizing/biasing

Optimize for centering, yield

Optimization works well here

Gain 60dB
UGF 111MHz
Phase 60deg
Slew 2V/us
CMRR: 60dB
PSRR: 70dB
THD: 1%
...

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Some Commercial Successes

- Ex: Sizing (and also layout) very useful for migration
- Can size, optimize for perform/yield, layout, migrate ...

STMicroelectronics result
[Shah, Dugalleix, Lemery DATE02]

180nm
Auto Sizing
Auto Layout
Area: ~9000 µm²
Power: 9.15mW

120nm
Auto Sizing
Auto Layout
Area: ~4000 µm²
Power: 1.1mW

[Source: Cadence]
Broad Landscape Emerged...

- **Simulation-based tools**
  - “SPICE-in-the-loop”
  - **PRO**: same setup as validation
  - **CON**: slowest to run; scaleup?

- **Analytical modeler tools**
  - “convex”, “smooth” etc
  - **PRO**: run fast, scale to big ckts
  - **CON**: long setup; accuracy?

Ex: Cadence Virtuoso ADE

Ex: Synopsys Titan AVP

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Core Layout Model: Design at 3 Levels

- **Devices** play role like gate-level cells in digital ASIC, but more complex, malleable; we need **device-generators**

- Macroscopic level, it's all more like floorplanning, placement, routing
Analog Layout: DeviceGen + Place/Route

- To first order, this is a *(very constrained)* place/route task...

- But with *very* complex generators for atomic pieces (devices)
Again, Some Commercial Successes...

Human resources comparison (normalized)

- Digital
- Analog B/E
- Analog F/E

Previous Design
New Design
Porting (Estimation)

Toshiba

Handcrafted

Automatic Place/Route

Courtesy: Neolinear, Cadence
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So, why is analog not yet a ‘solved’ problem...?
Pause, Reflect...

...then, I propose to commit Philosophy

(I warned you....)
Aggressive Philosophical Proposition...

- There are, in real world, only **2** kinds of EDA tools

...and you must figure out *what kind* you are building
Lessons Learned from First-Gen Tools

- **Things we got RIGHT**
  - Tools based on **optimization**
  - Models & setup for custom design are **critical synthesis IP**
  - Tools embedded in **same design flows** as manual ckt design
  - **Divide & conquer** (capture/synth/gen/P&R, etc) critical

- **Things we MISSED**
  - **Usage models** – how real people do real designs
Our 1st Generation of Sizing Synthesis Tools

- Built **Sizing Optim**
- Then **Constraint Mgr**
- Then **Statistical Centering**

**Expected Designer Interest**

- **Sizing**
- **Constraint Manage**
- **Statistical Center**

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Our 1st Generation of Sizing Synthesis Tools

Built Sizing Optim

Optimization Engine

Evaluation Engine

Then Constraint Mgr

Then Statistical Centering

Constraints

Statistical Center

Sizing

Actual Designer Interest

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1st Gen Synthesis Tools Revisited

Built **Sizing Optim**  

Then **Constraint Mgr**  

Then **Statistical Centering**

**Optimization Engine**

**Evaluation Engine**

**Constraints**

**Statistical Center**

**Actual Designer Interest**
Our 1\textsuperscript{st} Gen of Layout Synthesis Tools

- Built **Device Generators**
- And **Placer**
- And **Router**

Expected Designer Interest

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My 1st Gen of Layout Synthesis Tools

Built **Device Generators**

And **Placer**

And **Router**

**Actual Designer Interest**
Why? #1 Your Schematic is NOT What You Lay Out

- Map ckt to what can really work in layout
- Groups of devices w/ complex constraints
- Surprise: enormous pain here to get right; gen’s reduce layout time & reduce size (a lot)
Why #2: Curse of Analog Aesthetics...

- Consider thought experiment: I want 12 analog layouts
Why #2: Curse of Analog Aesthetics...

- Experimental method 11 layout experts & 1 CAD tool
Why #2: Curse of Analog Aesthetics...

- Probability $\to 1$, will get 12 *different* layouts, all *correct*
Why #2: Curse of Analog Aesthetics...

- Probability → 1, all humans think all other layouts look wrong
The Real *Reason* for Analog Aesthetics

- Why this remarkable, relentless focus on “my way” of layout?
- Aesthetics is often a surrogate for correctness
  - Not everything that matters in analog is robustly – or even *explicitly*, and *correctly* – represented in the design process.
- Consequence: Aesthetics used for insurance!

Hey, that looks *strange*, right?
Future Opportunity....
Context: Bifurcating Analog Space

Different kinds of design problems in 2 analog spaces

- **CHEAP analog**
  - Need the function && cheap
  - Don’t need 20M gates of logic

- **AGGRESSIVE analog**
  - Need function AND integration
  - Lowest-power + highest-volume

- **Pro/Con**
  - Cheap, fewer nm effects
  - Can’t integrate lots of gates

- **Pro/Con**
  - Low-power, access to 50M+ gates
  - nm grief is worse here
Today, most CHEAP ANALOG is mostly moving toward whatever is the LAST PLANAR CMOS NODE ~28nm

AGGRESSIVE ANALOG → 10nm
New Challenge: Nonplanar FinFET Devices

Which of these is not like the others?

- 180nm
- 90nm
- 45nm
- 16nm_FinFET

Courtesy Elias Fallon, Cadence Design, ISVLSI 2016
New Challenge: Nonplanar FinFET Devices

“Mature-node”

“Advanced node”

Courtesy Elias Fallon, ISVLSI 2016
The FinFet Challenge

- Devices are radically different, dominated by litho regularity
- Interconnect stack also different, very fine pitch for lower Metals

Source: Jan et al, “A 22nm SOC platform technology featuring 3-D tr-gate and high-k/metal gate, optimized for ultra low power, high performance and high density SOC applications,”, Prof IEEE IEDM, 2012.

FinFet Consequences...

- Custom analog cells look like **row-based layouts**...

Matching rules (dummies)
Density rules (FEOL, MEOL)
Gradient rules (for transition)
Coloring rules (routing)

FinFet Upside (Sort of...) for Analog Tools...

- 2001: 130nm
- 2005: 90nm, 65nm
- 2010: 45nm, 32nm, 22nm
- 2016: 14nm, 10nm, 7nm, 5nm

**Circuit Designer**

**Layout Designer**

**Cadence:** Layout Effort vs. Process Node

- **24x** the layout cost designing @ 7 vs 40nm

**Introduction of FinFets**

**Process Node (NM):**

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<th>40nm</th>
<th>28nm</th>
<th>16/14nm</th>
<th>10nm</th>
<th>7nm</th>
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Summary

- **Looking backward: Analog tools**
  - CAD = *Optimization* + constraints
  - Learned: aesthetics & usage matter

- **Looking ahead: Analog Tools**
  - Analog essential for *power/volume*
  - Huge opportunity to go at finFETs (pain)
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